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6. AUTHORS
James S. Im
Robert S. Sposili, compiler

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
The Trustees of Columbia University In the City of New York
1210 Amsterdam Avenue
New York, NY 10027-6999

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9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Coastal Systems Station, Dahlgren Division NSWC
6703 West U.S. Highway 98
Panama City, Florida 32407-7001
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This report describes new excimer-laser crystallization (ELC) techniques for producing high-quality Si films for AMLCD applications. These artificially controlled super-lateral growth (ACSLG) processes deliver crystalline silicon films with microstructures optimized for thin-film transistor applications. The ACSLG methods described herein include (1) a low-temperature method for producing grain-boundary-location-controlled (GLC) Si films on glass substrates, (2) a high-temperature method for producing single-crystal islands (SCI) on quartz substrates, (3) a realistic two-dimensional program for simulation of ELC, and (4) low-temperature sequential lateral solidification of Si films. Preliminary TFT devices have yielded near-record performance characteristics and demonstrate that the ACSLG materials are superior to existing materials for fabrication of TFTs. The sequential lateral solidification (SLS) process possesses two characteristics not found in any other technique: (1) it can produce the best material (single-crystal silicon films) for TFT devices, and (2) it does so directly on low-cost, low-temperature substrates. The impact of the SLS process will be to create a new materials/device technology: low-temperature single-crystal silicon TFTs, which will (1) displace conventional low- and high-temperature polycrystalline silicon TFT technology; (2) eliminate the need to utilize silicon-on-insulator (SOI) processes; and (3) ultimately enable the realization of highly integrated AMLCDs and system-on-glass products.

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# Excimer-Laser Crystallization of Si films

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Prepared by
James S. Im

Department of Chemical Engineering, Materials Science, & Mining Engineering
School of Engineering and Applied Science
Columbia University
New York, New York 10027

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Contract Number: N61331-94-K-0033

Prepared for Dr. G. Henderson
Naval Surface Warfare Center, Dahlgren Division
Coastal Systems Station
6703 West U.S. Highway 98
Panama City, Florida 32407-7001
ATTN.: Code RO53, Code SC13

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## I.A. EXECUTIVE SUMMARY

As a direct result of DARPA's support of Columbia's research program on excimer-laser annealing (ELA) during the past three years, we have succeeded in inventing, developing, and applying for intellectual property rights for a new family of ELA techniques that represent a leapfrog approach for producing high-quality Si films for AMLCD applications. These processes, which were no more than conceptual ideas just three years ago, have become robust methods that deliver crystalline silicon films with microstructures that are optimized for thin-film transistor applications. They are collectively referred to as the artificially controlled super-lateral growth (ACSLG) method, and were developed based on the fundamental understanding of ELC phase transformation scenarios we acquired through our previous efforts.

Specifically, the DARPA program enabled us to exploit our knowledge base of the ELA process in order to invent, develop, and optimize (1) a low-temperature method for producing grain boundary location-controlled (GLC) Si films on glass substrates, (2) a high-temperature method for producing single-crystal islands (SCI) on quartz substrates, (3) a realistic two-dimensional program for simulation of ELC, and (4) low-temperature sequential lateral solidification of Si films. We have achieved our objectives through controlled solidification of thin Si films using various means, such as simple photolithographic patterning or projection irradiation of the beam through a patterned mask.

As was originally envisioned, the program proceeded in a systematic and progressive manner; we have (1) characterized in detail the SLG phenomenon that forms the backbone of all ACSLG method, (2) developed realistic two-dimensional numerical simulation code to analyze the lateral solidification phenomenon, (3) developed and tested various patterning and alternative techniques to induce ACSLG, and (4) identified and optimized -- via experimental and numerical techniques -- the best approaches for producing ACSLG materials. The investigation has shown that all ACSLG methods have yielded results that exactly match the predictions based on our fundamental models of ELC phase-transformation scenarios. Our successes with the ACSLG processes are a direct consequence of our expertise in the fundamental aspect of the ELC processes (which we pioneered) and represents Columbia's unique contribution to the future of TFT technology.

The only difficulties that were encountered in the program were with respect to coordinating collaborative efforts with XMR and Xerox for fabricating TFT devices. Various internal reorganizations that transpired within these organizations have made the originally envisioned collaborative interactions, which were to take place during the third year of the contract, not a productive option. Subsequently, concerted effort was made in order to arrange a collaborative effort with a TFT team at Lawrence Livermore National Laboratory. With an appropriate contract modification and extension executed with encouragement and help from Dr. Henderson, we are now in the process of addressing this device-related component of the program. Nevertheless,

preliminary results using non-optimal ACSLG materials have already yielded near record performance characteristics and fully demonstrate that -- as expected based on device physics considerations and previous experimental results -- these ACSLG materials are superior to existing materials for fabrication of TFTs (i.e., improved both in the uniformity and the performance of the resulting devices).

It can be readily concluded that the sequential lateral solidification (SLS) process represents the singular and most potent outcome of the program in that this process is expected to revolutionize the field of TFT technology because it possesses two characteristics not found in any other technique: (1) it can produce the best material (single-crystal silicon films) for TFT devices, and (2) it does so directly on low-cost, low-temperature substrates in a rapid, simple, and technically non-demanding manner. It therefore can be developed into an economical and high-throughput production process.

The impact of the SLS process will be to create a new materials/device technology: low-temperature single-crystal silicon TFTs. Such a technology would (1) displace the inferior conventional low- and high-temperature polycrystalline silicon TFT technology; (2) eliminate the need for low-throughput, high-cost single-crystal silicon TFTs that utilize silicon-on-insulator (SOI) processes; and (3) ultimately enable the realization of highly integrated AMLCDs and system-on-glass products, in which various electronic components are monolithically incorporated onto a low-temperature glass (or plastic) substrate. Additionally, the process would be ideal for fabrication of intelligent displays and ultrahigh-resolution, low power consumption AMLCDs. The potential impact of the process is keenly reflected in the strong interest expressed by major U.S.-based and international groups engaged in TFT research and development. Currently, we are planning to work with other DARPA-funded research teams in the near future in order to implement and develop this revolutionary technology.

## I.B. OUTCOME OF THE CONTRACT

- **GLC Si Films on Low-Temperature Substrates.** We have successfully produced grain boundary location-controlled (GLC) Si films on low-temperature glass substrates. By (1) reducing the number of grain boundaries (which the majority carriers must overcome within the active channel portion of the devices), as well as (2) eliminating the variation in the number of such grain boundaries in the region, the GLC microstructure is well suited for TFT devices. That is, these GLC poly-Si films would enable fabrication of TFT devices in which only one perpendicular grain boundary is located within the active-channel region of the TFT.

- **SCI on Quartz Substrates.** We have successfully produced single-crystal islands (SCI) on quartz substrates. These single-crystal islands, each of which is sufficiently large for complete inclusion of a TFT device, enable the fabrication of single-crystal TFT devices on quartz substrates. This method, however, is limited in that it requires high substrate temperatures. This precludes the use of Si films on glass substrates but can be utilized in conjuction with quartz substrates.

- **Single-Crystal Si on Low-Temperature Substrates.** We have successfully produced single-crystal regions and islands on low temperature substrates for TFT devices -- the ultimate microstructural configuration for high-performance TFT devices. These single-crystal islands and regions, which are sufficiently large for complete inclusion of a TFT device, enable us to fabricate single-crystal TFT devices on low-temperature glass substrates (or for that matter, other low-temperature substrates such as plastics). The resulting performance and uniformity of the devices on these materials are expected to be at or near the level of single-crystal-based transistors. As such, it is expected to establish itself as the most suitable material for highly integrated, ultra-high-definition, intelligent AMLCDs and would rapidly enable the actualization of the "system-on-glass" concept.

- **SLS Process.** We have successfully developed the SLS process that involves (1) excimer-laser irradiation through a patterned mask via a projection-based beam delivery system and (2) precisely controlled translation of the sample with respect to the beam. The SLS process possesses characteristics that are well suited for adaptation of the process as a very attractive production method in that it (1) can be a high-throughput and rather parameter-insensitive (i.e., processing-friendly) technique, (2) need not involve irradiation in a vacuum or controlled atmosphere, (3) need not involve any preheating of the substrate, and (4) need not

involve photolithographic patterning of the Si films. We have demonstrated all of the above characteristic of the SLS process.

- **ACSLG Process.** Photolithographic patterning and projection-based excimer-laser irradiation processes are used to produce the above materials. This is called the artificially-controlled super lateral growth (ACSLG) process. All ACSLG techniques involve irradiation of an Si film at an energy density that is sufficient to induce complete melting of the film at--*and only at*--predesignated locations within the film. As the film cools, lateral solidification commences from the solid-liquid interface at the boundary between the completely and incompletely molten regions into the molten areas. By properly harnessing the process, it is possible to manipulate the microstructure of resulting Si films. It has been shown that the ACSLG processes are highly manufacturing-friendly in that, in contrast to conventional ELA methods, they possess wide processing windows and produce optimally microstructured materials.

- **2D Numerical Program.** We have succeeded in developing a two-dimensional numerical program that is capable of realistic simulation of excimer-laser-induced melting and solidification processes. The program also provides, indirectly, important information pertaining to the final microstructures.

- **TFT Devices on ACSLG Materials.** Performance characteristics of the TFT devices, which are fabricated on ACSLG materials, are being measured. This represents the *only* component of the original program in which we have encountered difficulties. The situation is currently being rectified via a collaborative effort with LLNL group. The original plan of making TFTs with Xerox and XMR was not pursued due to internal restructuring and changes at these companies.

## II.A BACKGROUND INFORMATION

### INTEGRATED ACTIVE-MATRIX LIQUID-CRYSTAL DISPLAYS

One important aspect of active-matrix liquid-crystal displays (AMLCDs) is the fact that the capability to fabricate thin-film-transistor (TFT) devices on a transparent substrate lies at the heart of the technology [II.A. 1]. This presents AMLCD technology with an unusual opportunity to aspire and become much more than a "display" technology. The idea here is this: it is possible for one to readily fabricate additional transistors to execute various electronic functions -- those that would otherwise be handled by separate LSI and VLSI circuits -- on the periphery of the display [II.A. 2]. Since this can be done, in principle, with no -- or a minimal number of -- additional processing steps, substantial cost reduction is possible and significant value can be added to the final product.

Doing so, and doing it well can ultimately lead to "system-on-glass" products in which the entire electronic circuitry needed for a product is incorporated directly onto a glass substrate. The situation should register as a significant one since this means that integrated active-matrix liquid-crystal displays (IAMLCDs) will bypass conventional Si-wafer-based products and may lead TFT technology to the level at which it may potentially compete directly against Si-wafer-based monolithic integrated circuits.

### LOW-TEMPERATURE CRYSTALLINE Si TFTS ON GLASS SUBSTRATES

The above-mentioned evolutionary path of the AMLCD technology is where the major materials-related issues come into play. Currently established TFT devices -- transistors that utilize hydrogenated amorphous Si films (i.e., a-Si:H TFTs) -- have clear performance limitations that make them unsuitable for IAMLCDs. In order to actualize IAMLCD products, crystalline-Si-film-based (be it microcrystalline, polycrystalline, or single-crystal) TFTs must be employed [II.A. 1]. Furthermore, in order for IAMLCD technology to realize its full potential and impact the flat-panel display (FPD) field in a substantial manner, it is necessary to fabricate high-quality crystalline Si TFTs (i.e., devices with high and uniform performance characteristics), and to do so directly on large and low-cost glass substrates [II.A. 3]. This is a challenging task as a consequence of (1) the amorphous nature of glass substrates, and (2) the inability of the substrates to tolerate sustained high processing temperatures.

The use of crystalline-Si TFTs as pixel transistors will also bring about additional benefits that include a higher aperture ratio, lower power consumption, and faster response times.

For these reasons, development of a good processing method to produce high-quality crystalline Si films on glass substrates remains an important and relevant issue. By and large, the main thrust of the investigations is on developing glass-substrate-compatible methods to crystallize as-deposited a-Si films. To this end, solid-phase crystallization -- with or without a self-implantation step -- and

excimer-laser-induced crystallization of a-Si films can be identified as being the two major approaches that have been investigated in the past.

**THE EFFECT OF GRAIN BOUNDARIES ON TFT DEVICE PERFORMANCE**

The profound effect of high-angle grain boundaries on the transport properties of polycrystalline Si films, as well as on the electronic properties of polycrystalline-Si-based TFT devices has long been investigated and well-recognized [II.A. 4,5]. Not surprisingly, grain boundaries do not possess any beneficial qualities, and the presence of grain boundaries within the active-channel portion of a TFT device leads to a degradation in its performance.

The performance degradation of the devices arises from the presence of a high density of trapping states that lie within the band gap. The traps exert a major influence on nearly all aspects of device performance: they lead to an increase in threshold voltage, a decrease in subthreshold slope, a decrease in field-effect mobility, an increase in leakage current, and poor device stability. The physical origin of the trapping states at the grain boundaries is generally thought to be associated with the presence of dangling and strained bonds. Hence, the hydrogen passivation technique has been applied successfully to improve the device performance of polycrystalline-Si-based TFTs [II.A. 5,6]. Also, clever device design schemes have been developed in order to cope with and further improve the performance of the devices [II.A. 7]. It is noted, however, that these treatments amount to partial and cumbersome -- but necessary -- remedies, which fail to eliminate the intrinsic problems that originate from the grain boundaries located in the active-channel portion of polycrystalline-Si-based TFTs.

A number of recent investigations clearly reveal in quantitative detail the intimate association between the number of grain boundaries within the active-channel portion of a TFT and the resulting performance of the device [II.A. 8, 9]. Simply put, the more grain boundaries there are in the active-channel region, the poorer the device performance. It is therefore tempting to identify large-grained polycrystalline Si films as an ideal material for TFT devices. However, the situation is a bit more complicated because as the average grain size increases, variations in the number of grain boundaries within the active-channel region can, on a normalized basis, become correspondingly greater, and progressively worsen the uniformity of the devices. The uniformity of all TFTs in general, and the leakage current uniformity of the pixel-controlling transistors in particular, is an important issue that must be properly and optimally addressed in order to ensure high-yield processing in the actual production of AMLCDs. The moral of the story is simple: a conventional large-grained polycrystalline Si film (which possesses randomly located grain boundaries) makes for a non-ideal TFT material.

One conceptually straightforward way to overcome the above dilemma and deal with the performance/uniformity optimization issue would be to engineer and utilize polycrystalline Si films with large-grained and grain-boundary-location-controlled microstructures (i.e., eliminate the random aspect of the microstructure of conventional polycrystalline Si films). The devices that are fabricated on such grain-boundary-location-engineered materials would likely possess both higher performance and more uniform device characteristics than those that are

fabricated on conventional polycrystalline Si films. Figure II.A.1 illustrates various microstructural configurations within the active-channel portion of a TFT.

If we permit ourselves to take one step further in the general direction of engineering the microstructure of the active-channel regions, we invariably arrive at the configuration that can be readily identified as being the best material for TFT devices: Si films devoid of any grain boundaries within the active-channel portion [II.A. 13]. Here, the entire film need not be a single crystal; all that is required is to produce a film that has in it a number of single-crystal (i.e., grain-boundary-free) regions that are located in the active-channel portion of the TFTs [Fig. II.A.1]. When such a level of materials development is reached -- provided that commensurate advances in low-temperature device fabrication techniques have also been made (e.g., proper self-aligned doping of source and drain regions, formation of quality oxide layer, etc.) -- TFT-based large-area-electronics would be well-positioned to make a strong impact on the electronics market, since the performance characteristics of the resulting devices could presumably approach and rival those of the Si-wafer-based transistors or the TFTs fabricated on expensive silicon-on-insulator (SOI) materials [II.A. 14,15,16]

**PROCESSING ISSUES**

One of the most important points to note regarding the processing of crystalline Si films on glass substrates is the constraints that are imposed by the inability of the glass substrates to withstand high processing temperatures [II.A. 1]. This limitation exerts a profound influence on many aspects of materials preparation and subsequent device-fabrication procedures.

To this end, it is instructive to remind ourselves that the availability of large and inexpensive glass substrates, and the ability to manufacture TFT devices with uniform device characteristics on these high-temperature-intolerant substrates were the crucial factors behind the emergence and domination of a-Si:H-TFT-based AMLCDs -- and the factors that will likely continue to play just as critical roles for the future of crystalline-Si-TFT-based IAMLCDs. In other words, it appears imperative that the process by which high-quality crystalline Si films are prepared must at least be compatible with any glass substrates, and preferably compatible with low-temperature glass substrates [II.A. 3]

The corollary of the previous statement is that in order for high-quality crystalline-Si-TFT-based IAMLCD technology to become more than just a niche and/or transient player, the materials and device fabrication processes should not require quartz substrates, single-crystal Si wafers, nor SOI materials. The techniques that make use of such materials will eventually have to confront the negative consequences of utilizing size-limited and comparatively very costly substrates. (Unfortunately, in contrast to the conventional microelectronics industry, here one does not have the luxury of tapping into the well-known scaling law, and countering such a set-back by producing larger quantities of much-smaller displays on better but more-costly substrates).

Furthermore, a desirable processing method must possess the manufacturing-related virtues that are always sought in any production-worthy process, and that are instrumental in determining the eventual steady-state survival of the process in this brutally cost-competitive industry. This means that the method should not involve many processing steps, could be implemented with preexisting industrial infrastructure and equipment, should possess high throughput and yield rates, and should ultimately be cost-effective.

The methods discussed in the following sections are compatible, to varying degrees, with the above constraints. In each case, one starts with a-Si films that are deposited via various means onto glass substrates which may have been coated with a thin $SiO_2$ buffer layer. Low-pressure chemical vapor deposition (LPCVD) and Plasma-enhanced chemical vapor deposition (PECVD) methods represent two production-proven ways of depositing a-Si films on glass substrates [II.A. 1,5]. As-deposited PECVD a-Si films contain high concentrations of hydrogen atoms which must be annealed out, if optimal results are desired, before any of the crystallization methods are employed.

**EXCIMER LASER CRYSTALLIZATION OF a-Si FILMS**

In recent years, the use of excimer lasers for crystallizing a-Si films has established itself as the chosen glass-substrate-compatible means of preparing crystalline Si films for production [II.A. 45,46,47,48,49]. The method capitalizes on the power and versatility associated with an excimer laser -- a piece of equipment that is in the process of establishing itself as a serious manufacturing tool. In excimer-laser crystallization (ELC) of a-Si films, it is the fortuitous combination of the small thermal mass of Si films and the unique capability of an excimer laser to impart a high-energy pulse (up to tens of Joules per pulse) over a short pulse duration (tens of nanoseconds) at a wavelength that is highly coupled to the material (interband-transition-promoting UV wavelength) that helps to first induce and then confine high temperatures in the near-surface region; this in turn makes the process fully compatible with a variety of low-temperature glass and plastic substrates.

In distinct contrast to solid-phase crystallization of a-Si films, in which a-Si is directly converted to crystalline Si under isothermal conditions, ELC of a-Si corresponds to a highly transient process which occurs in an open system, and which *must* involve melting and solidification of the Si films. This being the case, ELC is actually not a low-temperature process per se; instead, it is a rapid melt-mediated crystallization process that takes advantage of the spatial and temporal localization of the heat-affected region. Here, the participation of the liquid phase can be readily identified as being the key ingredient of the process; it is the high interfacial velocities that are attainable with melting and solidification [II.A. 50] that enable the whole process to proceed within time scales which otherwise could not be accomplished via sluggish solid-state transformations [II.A. 51].

The short-lived participation of the liquid phase in a rapidly changing environment, along with the thin-film nature of Si, makes possible the occurrence of rather varied and complicated transformation scenarios.

(i.e., a proper consideration must be given to the possibility of various transformation kinetic paths and competitive kinetics [II.A. 52].)

**PHASE TRANSFORMATION SCENARIOS**

Before we delve into the details of the solidification scenarios, there are two important points to note regarding the physical configuration of the samples: (1) Si films are typically very thin (ranging from a few tens of nanometers to a couple of hundred nanometers), and (2) the films rest on top of an $SiO_2$ surface. The chemical stability and amorphous nature of $SiO_2$ basically make its surface a nonparticipating entity as far as the actual interface-led transformation is concerned. Its main duties are to serve as a stable surface, which mechanically supports the film, and as the medium in intimate physical contact that effectively conducts the heat away.

A few years ago, through the combined use of a melt-duration analysis conducted with an *in situ* transient reflectance technique and a microstructural analysis conducted using transmission electron microscopy, the basic transformation mechanisms that are involved in single-pulse irradiation of LPCVD a-Si films have been definitively identified [II.A. 53]. (The results are summarized in Table II.A.1, and TEM micrographs of the single-pulse-irradiated films are shown in Figure II.A.2.) The findings reveal that there are two major regimes (i.e., a low-energy-density regime and high-energy-density regime) and an important subregime that can be recognized based on the dependence of grain size and the melt duration as a function of the incident energy density. The microstructures observed in the low-energy-density regime, where the grain size increases with increasing energy density, are shown to be associated with explosive crystallization followed by partial melting and regrowth of the film. The situation in this low-energy-density regime is similar -- but not identical -- to that encountered in pulsed laser annealing of ion-irradiation-amorphized Si surface layers. The high-energy-density regime, where the grain size is very small and is nearly independent of the incident energy density, is explained by the complete melting of the film, where substantial supercooling takes place before the onset of solidification commences via copious nucleation and subsequent growth of solids [II.A. 54]. (Earlier investigators may have incorrectly interpreted this regime as being associated with ablation of the film.)

An important subregime that produces the largest grain sized polycrystalline Si was discovered to take place within a narrow experimental window at the transition between the two major regimes. This phenomenon, referred to as the super-lateral growth (SLG) phenomenon, was explained in terms of liquid-phase regrowth from the surviving solid seeds at the bottom of the oxide interface when near-complete melting of the film occurs. The phenomenon has subsequently been theoretically analyzed in terms of the interface response function of the solid, the nucleation kinetics of the solid, and the transient lateral thermal profile near the solid-melt interface [II.A. 55]. (We will elaborate more on this phenomenon when we later discuss a new type of excimer-laser-crystallization process.)

In addition to the above basic scenarios, other noteworthy and unique observations include the effect of multiple-pulse irradiation at energy densities just below the complete-melting threshold and the amorphization of ultra-thin Si films [II.A. 56] upon complete melting and subsequent deep supercooling (> 500 °C) of the films [II.A. 57].

A systematic experimental investigation on the multiple-pulse-induced grain-enlargement phenomenon observed by a number of investigators [II.A. 58, 59, 60] reveals that the phenomenon corresponds to an unusual case of melting-and-solidification-induced microstructural evolution [II.A. 59]. It can be further shown that the phenomenon is apparently similar to -- but is physically quite distinct from -- conventional normal or secondary grain-growth processes, as it does not involve free-energy-reduction-driven motion of grain boundaries [II.A. 61,62]. A proposed model [II.A. 59] that invokes a complete melt-through of the film occurring mainly at and near the grain boundaries, and the effect of the interfacial energy anisotropy suggests that the microstructural evolution (1) is sensitive to the initial orientation distribution of the starting polycrystalline Si films, and (2) involves dynamic participation of all the grains. The model also predicts that the process would eventually lead to development of large-grained polycrystalline Si films with restricted crystallographic textures [II.A. 60].

**CONVENTIONAL EXCIMER-LASER CRYSTALLIZATION PROCESSES**

The mainstream approaches for applying excimer lasers to the crystallization of Si films can be divided into two categories: multiple-pulse-based and single-pulse-based. Of these, the multiple-pulse-based scanning method represents the conventional approach that is expected to be adopted as the first-generation ELC process for crystallizing a-Si films on glass substrates [II.A. 58,63]. The salient features of this approach include thorough homogenization of the incident beam using a multi-lenslet/mirror type homogenizer, irradiation of the samples at high pulse frequencies (up to ~100 Hz), shaping of the beam into high-aspect-ratio rectangles (up to 1:20), and scanning of the beam at high beam-translation rates (up to ~1 cm/s).

During the past several years, detailed parametric investigations on the multiple-pulse-based scanning method have been carried out by the Xerox PARC group on the dependence of TFT characteristics on process conditions [II.A. 58]. The study reveals unambiguously that while high-performance devices are obtained with irradiation conditions that produce large-grained polycrystalline materials, such performance improvement is accompanied by degradation in the materials and device uniformity. This observation, along with the fact that the microstructures and device performance vary sensitively within this processing window, leads one to conclude that the proper way of employing this method corresponds to irradiation of the films at low energy densities, in which the process leads to small-grained materials but is relatively insensitive to the spatial and pulse-to-pulse energy density fluctuations in the incident beam.

With the advent of the very high power excimer lasers (up to 50 J/pulse) that are now available in the commercial laser market, the single-pulse-based approach may be considered a viable alternative to the multiple-

pulse scanning method. The idea here is to crystallize a-Si films using a single pulse (or a few pulses) over a large area -- preferably the entire area of a single display unit within a glass substrate. Afterwards, the beam is moved (i.e., stepped) to the next display unit upon which the whole process is repeated. The process is physically simpler, and is potentially more attractive than the multiple-pulse-based scanning method. It is worthy of consideration for the following reasons: (1) it may be more controllable than the scanning method since there are fewer processing variables; (2) the beam can be thoroughly homogenized using a number of different techniques; and (3) very high throughput rates can be expected from the approach. Once again, crystallization should be conducted within the low-energy-density regime where the microstructure is fairly insensitive to variations in the incident energy density and within which small-grained polycrystalline Si films are obtained [II.A. 53].

One can thus fairly accurately summarize the current situation involving conventional ELC of a-Si as being centered on producing small-grained Si films with an acceptable level of microstructural uniformity using rudimentary irradiation techniques. Although the resulting small-grained polycrystalline films may initially be adequate for integrating the first-generation driver circuits, the TFT device performance characteristics obtained from these small-grained materials are rather poor as they do represent the lower end of the performance scale associated with crystalline Si films. As such, these materials likely would not enable further integration of more-demanding circuitry. Moreover, these conventional ELC approaches would likely not lead to better-performance-inducing high-quality crystalline materials in that the large-grained materials are obtained (1) only within a narrow processing window [II.A. 53,55,58] where the materials and device uniformity is unforgiving to small variations in incident energy densities, and (2) the resulting large-grained polycrystalline Si films have random microstructures in which the grain boundaries, inevitably, are located in an unpredictable manner [II.A. 53,58,59,60].

## II.B. ARTIFICIALLY CONTROLLED SUPER LATERAL GROWTH PROCESSES:
NEW EXCIMER-LASER CRYSTALLIZATION METHODS

Motivated, in part, by the apparent compromises and physical limitations associated with the conventional excimer-laser and solid-phase crystallization approaches, we have developed -- through this DARPA-sponsored program -- a new generation of ELC processes. These processes are collectively referred to as the artificially controlled super-lateral growth (ACSLG) method, as they have been conceived as a result of analyzing the solidification scenario behind the super-lateral growth phenomenon.

The ACSLG method is based on the spatially controlled manipulation of the excimer-laser-induced solidification of an Si film. It seeks to control the resulting microstructure by inducing complete melting of selected regions of the Si film via projection irradiation through a patterned mask or via use of a photolithographic patterned anti-reflective coating or absorption layer. Common to all ACSLG techniques is the irradiation of an Si film at an energy density that is sufficient to induce complete melting of the film at--*and only at*--predesignated locations within the film. As the film cools, lateral solidification commences from the solid-liquid interface at the boundary between the completely and incompletely molten regions into the molten areas. This in turn leads--as a simple consequence of microstructural development during solidification--to microstructures that consist of large and nonequiaxed grains (i.e., grains that are elongated in the direction of solidification). The ACSLG processes are highly manufacturing-friendly in that, in contrast to conventional ELA methods, they possess wide processing windows and produce optimally microstructured materials.

ACSLG methods can provide large-grained and grain-boundary-location-controlled Si films on low-temperature glass substrates, large single-crystal islands on high-temperature quartz substrates, and single-crystal regions on low-temperature glass substrates. The attainment of single-crystal material via an excimer-laser-irradiation method, in particular, will lead to the creation of a new materials/device category: *low-temperature single-crystal-Si-based TFT devices*. In addition to IAMLCDs, such a material would presumably be useful for a number of other large-area circuits and silicon-integrated-circuit applications, including megabit static random-access memory (SRAM), image (and other) sensors, high-resolution active-matrix electroluminescent displays (AMELDs), and less-demanding SOI devices. As well, the process appears to be uniquely suited for, and may at last enable, the development of uncompromised three-dimensional integrated circuits.

## II.C. GRAIN BOUNDARY-LOCATION-CONTROLLED Si FILMS.

### GLC-Si SECTION SUMMARY

Based on the previously elucidated super lateral growth phenomenon, we have developed a new excimer-laser crystallization method that produces large-grained and grain-boundary-location-controlled Si films on $SiO_2$ and which possesses a wide processing window. A patterned $SiO_2$ capping layer on top of Si films is utilized as an anti-reflective coating in order to induce artificially controlled super-lateral growth upon being irradiated with a single excimer-laser pulse. For a simple $SiO_2$ stripe pattern, the occlusion among the laterally and directionally solidifying grains permits the eventual development of elongated parallel grains with a single perpendicular grain boundary, which is localized in the middle of the completely melted regions -- provided that the width of the completely molten region is sufficiently narrow so as to avoid the nucleation of solids in the supercooled liquid.

### TECHNICAL MOTIVATION FOR GLC-Si FILMS

In order for thin-film-transistor (TFT) based integrated active-matrix liquid-crystal displays (AMLCDs) to impact display applications in a substantial manner, the following well-defined materials issues must be properly and optimally addressed: First, the microstructural integrity of the crystalline Si films on which the TFT devices are fabricated must be such that the resulting devices possess, in a reproducible manner, good electronic performance *and* uniform device characteristics. Extensive investigations have revealed the detrimental effects that grain boundaries have on the electronic characteristics of poly-Si TFT devices [II.C. 1]. Accordingly, in order to improve both the performance and uniformity of the devices, one must (1) reduce the number of grain boundaries (which the majority carriers must overcome within the active channel portion of the devices), as well as (2) eliminate the variation in the number of such grain boundaries in the region [II.C. 2]. In addition, it is imperative that the very procedures by which the films are processed must be technically undemanding as well as economically competitive.

Unfortunately, the currently available approaches do not satisfactorily address the above demands, and consequently, the need for finding a solution that capably deals with such requirements exists. The GLC approach addresses the above demands by producing large-grained and grain-boundary-location-controlled (GLC) Si films and does so in a processing-friendly and experimental-parameter-insensitive manner.

### PROCEDURAL DETAILS

As far as the sample configuration is concerned, a photolithographically patterned $SiO_2$ layer (stripe patterns with widths of 2 μm or 10 μm, and a separation distance of 1.5 μm) on top of a LPCVD a-Si film (1,000 Å or 2,400 Å) was chosen to induce a lateral variation in the amount of energy absorbed by the Si film, which was deposited on top of a thickly oxidized (2 μm) Si substrate. A particular $SiO_2$ layer thickness of approximately 500 Å was selected in order to induce the antireflective

coating effect [II.C. 6] *while* minimizing the conductive cooling of the a-Si film by the capping layer that inevitably occurs during the initial heating period. (As expected -- and noted previously [II.C. 4] -- the critical incident energy densities required to completely melt a continuous Si film showed a substantial difference for oxide-capped and capless Si films: 300 $mJ/cm^2$ and 395 $mJ/cm^2$ at room temperature (280 $mJ/cm^2$ and 350 $mJ/cm^2$ at 150 °C) for capped and uncapped 1,000-Å Si, respectively, and 585 $mJ/cm^2$ and 720 $mJ/cm^2$ at room temperature for capped and uncapped 2,400-Å Si, respectively.)

The samples were irradiated at various energy densities and substrate temperatures inside the hot-stage-equipped vacuum chamber with a 30-nanosecond, 308-nanometer XeCl excimer laser pulse. After irradiation, the microstructures of irradiated films were analyzed using Transmission Electron Microscopy (TEM) (or using Scanning Electron Microscopy (SEM) after the films were subjected to a defect etching process).

**RESULTS**

TEM micrographs illustrated in Figure II.C.1 show the prevalent and representative microstructures of single-pulse crystallized Si films with a 2-μm-wide patterned capping layer (separated by 1.5-μm cap-free region) corresponding to incident energy densities of 190 $mJ/cm^2$, 290 $mJ/cm^2$, 340 $mJ/cm^2$, and 385 $mJ/cm^2$ at a substrate temperature of 150 °C. Figure II.C.1a shows the typical small-grained poly-Si films that are obtained when the incident energy density corresponds to the value that induces partial melting in both the capped and uncapped films (i.e., within the low-energy-density regime [II.C. 4] for both configurations). Careful inspection of the capped and uncapped portions of the film reveals that slightly larger grains are obtained -- for this particular energy density -- under the capped region than within the uncapped region.

Figure II.C.1b (as well as 1c) shows the GLC microstructure, which is obtained when the incident energy density is such that it leads to complete melting of the oxide-capped films but leads only to partial melting of the uncapped films (i.e., corresponds to the low-energy-density regime for the uncapped films, but corresponds to the high-energy-density for the capped films [II.C. 4]). The GLC microstructure consists of elongated and laterally columnar grains that originate from the unmelted portions of the film and which meet each other at the center of the patterned area. Not all of the grains that originate from the small-grained region survive the journey to the center, as a significant number of grains are quickly occluded, particularly near the onset of growth. As a result, large and elongated grains are obtained near the central region. The quantitative analysis of the GLC microstructure (Figures II.C.3a and 3b) clearly reveals such a non-random aspect -- especially within the central area -- of the material. The apparent uniformity of the GLC microstructure was excellent as the entire membrane that was inspected revealed the absolutely uniform microstructural pattern; this observation, along with the wide range of the energy density within which the GLC microstructure is obtained, directly attests to and bodes well for the potential applicability of the process.

Figure II.C.1d shows the primarily fine-grained microstructure (but

which also contains periodically arranged larger grains) that is obtained when the incident energy density corresponds to the value that induces complete melting of Si films in *both* the capped and uncapped configurations (i.e., within the high-energy-density regime [II.C. 4] for both configurations).

The most important point that can be made regarding the interpretation of the origin of the above microstructures is the fact that they correspond precisely to the very microstructures that can be anticipated based on the solidification scenarios and transformation analyses that were formerly presented [II.C. 4,5]; that is to say, these microstructures result, in a straightforward manner, from achieving various combinations of partial and complete melting of the Si film for the $SiO_2$ capped and uncapped regions. For example, the microstructure shown in Figure II.C.1a can be readily identified as corresponding simply to the microstructure obtained when partial melting and vertical regrowth of Si films occurs for both regions.

Likewise, the microstructure shown in Figures II.C.1b and 1c corresponds to the case in which partial melting occurs in the uncapped portion of the Si film while complete melting occurs in the capped region of the film; this is the necessary condition for the ACSLG process and the corresponding experimental parameter range within which this condition is achieved is the ACSLG processing window. If and when such a condition is satisfied, controlled super-lateral growth always initiates from the unmelted regions of the film and directionally proceeds into the completely molten portion of the film. (It is worthwhile to note here that the use of a patterned $SiO_2$ layer to induce the conditions needed for ACSLG processes represents but one of the several methods -- many of which can lead to a large ACSLG processing window -- that can be employed for the task [II.C. 3].)

For the situations corresponding to 1b and 1c, the two solidification fronts originating from the two unmelted sides eventually impinge on each other (i.e., the width of the completely molten region is narrow enough so as to avoid deep supercooling and subsequent nucleation of solids within the middle of the region) and form a well-defined grain boundary that is located precisely at the center of the molten region.

On the other hand, and as expected, Figure II.C.2a shows that -- for the substrate temperature and the film thickness combination of 400 °C and 2,400 Å -- the small-grained region appears within the completely molten region, as the width of the completely molten region is sufficiently wide (10 μm) such that the temperature of the liquid in the middle portion of the completely molten region became *low enough for a long enough time interval* so as to trigger the spontaneous nucleation of solids within the region. This being so, the width of the small-grained region decreases with increases in the substrate temperature [II.C. 7] and eventually disappears, as can be observed in Figure II.C.2b; this observation is commensurate with the previous explanations that were provided regarding the effect of variations in experimental parameters on the extent to which lateral growth can proceed [II.C. 5].

Figure II.C.1d corresponds to the case in which complete melting of the entire film occurs, leading subsequently to the solidification via nucleation-initiated transformation for the both capped and uncapped

regions. However, because nucleation of solids is triggered at an earlier time for the uncapped portion of the film, some lateral growth is observed -- as evidenced by the larger grains near the pattern boundaries. This lateral growth presumably initiates from the solids that nucleated earlier within the uncapped portion of the film, and proceeds into the capped portions of the film until nucleation is triggered within that region. Such a difference in the nucleation initiation time is expected in the present case because (1) the Si film under the $SiO_2$ capping layer rises to a much higher temperature since it absorbs more of the incident energy and (2) the thin capping layer, whose thickness is well within the characteristic thermal diffusion length (i.e., small thermal mass) and which initially acts as a heat sink during the heating period, will eventually act instead as a heat source during the conductive cooling period. These factors will both work to delay, compared to the uncapped portions of the film, the time at which the liquid temperature underneath the capping layer reaches the nucleation triggering range.

As to the specific use of the GLC microstructure for TFT devices, Figures II.C.4a and 4b schematically illustrate the possible placement of the active channel portion of the device to coincide with the GLC region of the film. Figures II.C.4a and 4b show TFT devices with one perpendicular grain boundary and no perpendicular grain boundaries, respectively, within the active-channel region of the devices.

The important point to note here is that it is in fact readily possible to fabricate such devices because: it is possible to control precisely the location of the GLC region within the substrate through the photolithographic technique; the dimensions of the achievable GLC region are sufficiently large to accommodate conventional and future device structures; and the microstructure of the GLC region, particularly near the center of the region, is highly uniform.

## II.C. SINGLE-CRYSTAL Si ISLANDS ON $SiO_2$.

### SCI SECTION SUMMARY

We have succeeded in developing a single-pulse-based excimer-laser crystallization technique that transforms photolithographically patterned and $SiO_2$-encapsulated a-Si regions into single-crystal islands on $SiO_2$. The method utilizes the substantial super-lateral growth distances that are attainable at high substrate temperatures in combination with precise manipulation of the evolution of the solidification front in order to allow only one of the several grains that originate from the intentionally incompletely melted (i.e., the seed) portion of an island to pass through a constriction and propagate into the rest of the island. This converts the main portion of the island, which extends tens of microns in the lateral dimensions, into a high-angle-grain-boundary-free crystalline material, in so far as the size of the island is commensurate with achievable super lateral growth distances.

### TECHNICAL MOTIVATION FOR SCI Si

Thin-film transistor (TFT) devices on quartz substrates, which have been and are continually being manufactured for active-matrix liquid-crystal display (AMLCD) applications [II.D. 1,2], represent an important and viable approach within the field. The configuration is particularly attractive and cost-effective for those applications that require small AMLCDs since significant benefits would result from the simultaneous integration of driver and other peripheral circuits directly onto the substrate [II.D. 3]. This, in addition to the well-recognized benefit of employing established conventional semiconductor fabrication processes (as well as the technical difficulties that confront the development of low-temperature AMLCDs with integrated circuits [II.D. 4]) makes for a compelling case to further improve the approach.
High-temperature poly-Si TFT devices in their current form, however, suffer from intrinsic problems that originate from the random and defective microstructural nature of the starting poly-Si films [II.D. 1,2]: the main culprit here is the high density of high-angle grain boundaries in the films--the elimination of which represents, in our opinion, the best remedy for the problem.

### SCI PROCESS AND MATERIAL

In this section we describe the development of a high-substrate-temperature single-pulse-based excimer-laser crystallization (ELC) technique that utilizes an excimer laser pulse to convert as-deposited a-Si or poly-Si regions into high-angle-grain-boundary-free single-crystal islands (SCIs) on $SiO_2$. As the process requires a substrate temperature in excess of 1,000 °C, it is not suitable for Si films on glass substrates but is, on the other hand, readily applicable to Si films on quartz substrates. The purpose of this letter is to provide a technical description of the new method, to lend the conceptual framework and physical rationale behind the approach, and to deliver the experimental verification of the technique.

The SCI method described in this section constitutes one of several processes that are currently being developed in order to address and overcome the processing difficulties and materials limitations that are currently encountered and associated with the ELC of Si films. These processes are designed based on the physical insights that were gained from identifying and deciphering the super-lateral growth (SLG) phenomenon [II.D. 5,6] and are collectively referred to as the artificially controlled super-lateral growth (ACSLG) method.

At the crux of the ACSLG method lies the accurate control, via various technical means [II.D. 7,8], of the locations of the completely and incompletely melted areas of the film, so as to subsequently induce controlled lateral solidification from the incompletely melted areas into the completely melted regions. For the particular method presented in this letter (i.e., ACSLG/SCI), we further exploit (1) the readily available photolithographic capability to pattern the starting Si film and (2) high-substrate-temperature liquid-to-solid transformation characteristics, in order to actualize the single-crystal islands--each of which is more than large enough for a complete inclusion of a TFT device.

**PROCEDURAL DETAILS**

The first steps in the preparation of the samples involved deposition of 1,000-Å-thick a-Si and 1,000-Å-thick $SiO_2$ films sequentially on top of oxidized Si wafers or quartz substrates. The deposited a-Si/$SiO_2$ films were then patterned into a number of individual islands via conventional photolithographic procedures which included reactive-ion etching of the films in an $SF_6/O_2$ plasma. The basic shape of the pattern, which is shown in Fig. II.D.1(a), consists of two rectangular areas directly joined via a narrow bridge at the corners. The large square area represents the main "island" portion of the structure and the smaller rectangular area represents the auxiliary "tail" section. The lateral dimensions of the main region of the islands varied from 10x10 to 50x50 μm, while that of the tail section was fixed at 20x10 μm. The dimension of the bridge or the "bottleneck" region connecting the extension and the main area was also fixed at 5x3 μm. The patterned islands were encapsulated with 2,100-Å-thick $SiO_2$ via a plasma-enhanced chemical vapor deposition (PECVD) process. On top of the $SiO_2$-encapsulated samples, a second Si layer (1,200-Å-thick PECVD a-Si) was deposited and patterned to form 5x5-μm square patches. The positions of the patches were aligned so that each square was located directly above the tail section of an underlying island structure. Lastly, the square patches themselves were encapsulated with 1,700-Å-thick PECVD $SiO_2$.

The samples were placed inside a hot-stage-equipped vacuum chamber and irradiated with a single excimer-laser pulse (Lambda Physik COMPex 301, 30-nanosecond FWHM, and 308-nanometer wavelength). The hot stage was resistively heated, in less than three minutes, to a final substrate temperature which ranged between 1000 and 1200 °C. (as-deposited a-Si transformed to small-grained poly-Si via solid-phase crystallization during the ramping phase.) The sample temperature was directly monitored via a wafer-surface-bonded thermocouple [II.D. 9] and also by a digital infrared thermometer. In order to thermally stabilize the sample, it was held at the final substrate temperature for two minutes prior to irradiation. The initial set of experiments centered on

identifying the energy densities that were required to completely melt the first-level islands, without melting the second-level-shadowed (i.e., square-patch-masked) portion of the tail section, at various substrate temperatures. Subsequently, all experiments were conducted above the identified threshold. Scanning electron microscopy (SEM) and optical microscopy of defect-etched samples were performed in order to analyze the microstructure of the irradiated samples.

**RESULTS**

A subtle but significant feature of the excimer-laser-irradiated islands (Fig. II.D.1) is the excellent morphological integrity of the structure--the stability of which can be attributed to the presence of the oxide capping layer. In its absence, the agglomeration of liquid Si on an oxide surface occurs readily and consistently for the temperature/time scales that are involved in the current experiments.

As to the details of the solidification scenarios and the microstructures of the resulting islands, much can be elucidated from a systematic inspection of the optical micrographs of the defect-etched samples (Fig. II.D.2). First, Secco etching of the irradiated islands reveals that the irradiated islands contain a high density of planar defects, some of which are apparently reminiscent of the low-angle subboundaries observed in zone melting recrystallization (ZMR) of thin Si films [II.D. 10] and all of which originate presumably from the rapidly advancing solidification interface during the transformation.

In general, such defect patterns are known to be affected by the crystallographic orientation of the growing crystal with respect to the interface (which in turn is affected by the near-interface thermal profile) and also tend to be oriented in the direction that is normal to the interface [II.D. 11]. As such, they can reveal, in an indirect but consistent manner, the evolution of the solidification sequence. The overall spreading patterns formed by the defects in Fig. II.D.2, for example, reveal that the starting point for solidification of the islands, not surprisingly, corresponds to the beam-masked (i.e., shadowed) area within the tail section of the islands. The subsequent lateral growth of the grain within the main portion of the island proceeded to convert the region into a single--albeit defective--crystal that is entirely free of any random high-angle grain boundaries.

The above chain of events that is directly implied by the solidified microstructures corresponds to the melting and solidification scenario which was envisioned and under which the ACSLG/SCI process was designed to achieve; the shape and dimensions of the islands as well as the other specifics of the experiments were all dictated in order to induce the above transformation sequence. Due to the combination of several factors, including the pattern of heat flow, the occlusion phenomenon, and the likely shape of the interface during solidification, the possibility of two grains passing through the bottleneck region and propagating into the main portion of the island is remote and was, in fact, not observed.

The defect patterns shown in Fig. II.D.2(b), which correspond to the sample that was irradiated at the lower substrate temperature of 1,100 °C, demonstrate how random nucleation can become a destructive factor as the substrate temperature decreases. Here, it can be seen clearly that,

while the smaller island (20x20 μm) has successfully gone through the complete transformation, the adjacent larger islands (30x30 and 40x40 μm) have, in contrast, failed to do so due to the nucleation and subsequent growth of solids within the supercooled liquid--occurring well in front of the advancing interface. (The trend--i.e., incomplete transformation of the larger islands and complete transformation of the smaller islands--was observed consistently within the irradiated portion of the sample.) As the nucleation events potently and inevitably lead to creation of grain boundaries (presumably of the high-angle type) within the island, nucleation must be avoided.

**DISCUSSION ON THE SCI PROCESS AND MATERIAL**

We begin our discussion by enumerating the physical conditions that must be properly addressed in order to successfully and consistently implement the ACSLG/SCI process. First and foremost, it is essential that the basic ACSLG requirement regarding the control of complete melting and incomplete melting of respectively designated areas must be accomplished. In the present case, this translates into complete melting of the directly exposed region of an island and incomplete melting of the shadowed region.

Failure to meet either of the above-mentioned ACSLG conditions would mean that the irradiated islands would not be converted into single-crystal regions. The incomplete melting of the main island regions would result in small-grained (partial melting) or large-grained (near-complete melting) polycrystalline islands. The complete melting of the seed regions may, on the other hand, lead to the multiple-nucleation-initiated solidification of the islands which, once again, would result in a large-grained polycrystalline microstructure of the islands. An additional key requirement for the ACSLG/SCI process is to select the proper combination of island-size/substrate temperature so as to avoid possible nucleation of solids; the selection of a single grain through the constriction and the subsequent propagation of the grain into the main island is, in itself, a necessary but insufficient condition.

The physical phenomena that are responsible for dictating the ACSLG/SCI solidification sequences, and thus the resulting microstructures, are identical to those that were identified previously for the SLG phenomenon [II.D. 6]: the growth kinetics of the undercooled interface, the nucleation kinetics of solids in supercooled liquid, and the multi-dimensional thermal evolution during the heating, melting, and solidifying periods. An important and particular aspect of the situation encountered in the current experiments is that due to the high substrate temperatures, completely molten Si undergoes cooling at relatively low rates, and its temperature stays at or above the substrate temperature, which incidentally is higher than the estimated nucleation temperatures that are attained in rapidly quenched liquids [II.D. 12]. This in turn, means that the rates of appearance of nuclei in the completely melted and supercooled liquid can now be substantially lower in magnitude than those encountered in conventional ELC processes. Fundamentally, the situation also means that the transient/athermal nucleation mechanisms would not be factors and that the thermodynamically favored heterogeneous nucleation mechanisms can

now participate in the process because the mechanisms may no longer be kinetically bypassed.

The rate of growth is--in contrast to the rate of nucleation, which varies in a hypersensitive manner as a function of the temperature of supercooled liquid--a rather weakly varying function of the interfacial temperature [II.D. 13]. As a result, the ratio of nucleation rate to growth rate decreases rapidly as the liquid temperature creeps closer to the melting point. It is this very combination of the rates, which is accessible at near-equilibrium conditions, that fueled the design of the current experiments, since the combination permits substantial ACSLG distances to be achieved on a consistent basis. Furthermore, the hypersensitive dependence of the nucleation rate on the substrate temperature can be considered a major asset for the process in that the chance of random nucleation within an island can be simply and completely eliminated by trivially maintaining the substrate temperature at a sufficiently high value.

In the absence of any nucleation whatsoever, one can note the apparent similarity between the current approach and conventional directional solidification processes, which were investigated in order to manufacture SOI materials [II.D. 10]. Still, the extent to which the interface temperature undercools during the ACSLG/SCI process is expected to be significantly greater than that encountered in a typical directional solidification process; consequently, the growth rates involved in the ACSLG/SCI process are presumed to be correspondingly higher. Although it is not possible to experimentally determine the temperature of the interface during solidification, one can deduce that the lowest interface temperature encountered during the process must have, at least, been higher than the value that triggers the interface to amorphize, or the value that leads to the loss of epitaxial growth (i.e., fracturing in the crystallinity of the growing solid). Finally, we note that the problems which are prevalent in the near-equilibrium directional-solidification processing of ultra-thin Si films--such as lateral-thermal-stress-induced wafer warpage, agglomeration of molten Si, and thermal-mismatch-induced cracking of continuous Si films [II.D. 10]--are neither expected nor observed with the ACSLG/SCI method.

## II.E. NUMERICAL ANALYSIS OF EXCIMER-LASER-INDUCED MELTING AND SOLIDIFICATION OF THIN Si FILMS

### SECTION SUMMARY

We have developed an efficient two-dimensional numerical model, based on the finite difference method and utilizing the alternate-direction explicit scheme, that can simulate excimer laser melting and solidification of thin Si films on $SiO_2$. The model takes into account important aspects of the process such as undercooling and the temperature-dependent-velocity of the solidifying interface, supercooling of liquid Si, and the inert nature of the underlying oxide interface. We demonstrate the unique capability of the model by simulating spatially confined beam-induced localized complete melting of the irradiated portion of the film, and the ensuing lateral solidification, which initiates from the unmelted regions of the film into the completely molten area.

### MOTIVATION FOR THE TWO-DIMENSIONAL NUMERICAL MODEL

Previous experimental and theoretical analyses of the single-pulse and multiple-pulse excimer-laser irradiation of amorphous and polycrystalline Si films have established that excimer laser-induced crystallization (ELC) involves several varied rapid melting and solidification scenarios in which far-from-equilibrium conditions prevail [II.E. 1-4]. In particular, the process has been shown to involve lateral, as well as vertical, heat flow and phase transformations. Such two-dimensional thermal and solidification characteristics occur as a consequence of the films being very thin and the fact that they rest on top of an inert and amorphous $SiO_2$ surface [II.E. 1, 2].

The aforementioned features in turn make -- for those conditions that correspond to near-complete and complete melting of amorphous or crystalline Si films -- the transformation scenarios and the resulting microstructures that are encountered in the ELC process quite distinct from, and more varied than, those that are observed in pulsed-laser annealing (PLA) of Si surfaces [II.E. 5]. As well, they invalidate the use of the one-dimensional ELC numerical model that has been frequently utilized by a number of investigators [II.E. 6-8]; for these irradiation conditions, the vertical-regrowth solidification scenario that underlies their one-dimensional simulation results is incorrect. Additionally, close examination of a number of existing and related models [II.E. 6-17] reveals that they lack various capabilities and features that are needed in order to effectively accommodate and properly simulate the situations that are encountered in excimer-laser-induced melting and solidification of thin Si films on $SiO_2$.

In this section we describe details of a realistic transient two-dimensional numerical model and utilize the model -- which includes several of the important physical and transformation characteristics that are found in the ELC process -- in order to analyze the thermal response of a thin Si film on $SiO_2$ (Fig. II.E.1) when it is irradiated with a laterally tailored incident beam so as to induce spatially confined melting and solidification of the film. Such a situation is

encountered in a new category of ELC processes collectively referred as the artificially controlled super lateral growth method (ACSLG) [II.E. 18-21].

**DETAILS OF THE MODEL**

The spatial and temporal discretization and iterative computation of the following heat-transport equation in a manner consistent with the first order finite-difference method, and utilizing the Alternate-Direction Explicit (ADE) scheme [II.E. 22] constitutes the basis of our model; that is,

$$C_p(\phi,T)\frac{\partial T}{\partial t} = \frac{\partial\left(K(\phi,T)\frac{\partial T}{\partial x}\right)}{\partial x} + \frac{\partial\left(K(\phi,T)\frac{\partial T}{\partial y}\right)}{\partial y} + S_1(t) + S_2(t) \qquad (1)$$

with the *initial condition* T(0) = preheat temperature, and insulating boundary conditions at the top and the sides, where $C_p$ is the heat capacity, $K$ the thermal conductivity, $S_1$ the absorbed laser energy heat source function, $f$ the phase-identifier function, and $S_2$ the interface-localized latent heat function.

$S_1$ and $S_2$ correspond to two crucial source terms; $S_1$ deals with thermalization of the deposited laser energy, and $S_2$ treats the localized consumption (during melting) and generation (during solidification) of the latent heat, which takes place at the solid-liquid interface. The value of $S_1$ at a node within the irradiated portion of the film can take on a positive value during the irradiation when a non-negligible fraction of the nonreflected portion of the incident radiant energy reaches the node, and is at least partially coupled. Otherwise, $S_1$ is equal to zero (i.e., outside the irradiated area, or when no coupling occurs, or when a negligible fraction of the beam reaches the node, or subsequent to the beam duration, etc.). Because $S_1$ depends on the location (both vertical and lateral), temperature, and phase of a node, it enables the modeling of the position-dependent energy deposition process that occurs when a spatially tailored beam, whose energy density may be high enough to initiate and drive melting of the irradiated portion of the film, is incident on the film surface.

In contrast to $S_1$, which can principally be simultaneously activated in all of the effected nodes, *$S_2$ is active only in those nodes that contain the non-diffuse solid-liquid interface within their associated volume.* (By non-diffuse interface, we mean that the interface is computed to be localized and contained within a volume associated with a node -- i.e., one grid thick -- and that on either side of the node one finds nodes whose associated volume corresponds to liquid or solid.) The exact value of $S_2$ at an interface-containing node is proportional to the calculated local and instantaneous velocity of the solid-liquid interface within the volume associated with the node. This velocity, in turn, depends on the node temperature as dictated by the interface response function (i.e., systematic variation of the interface velocity as a function of the interfacial undercooling and overheating) that is built into the model.

The above description of the interface-localized nature of $S_2$ and the use of the interface response function within the model points to the important thermal and transformation-related computations that take place at those nodes that contain the interface within its associated domains. Within these nodes a gradual but rapid phase conversion (and linearly proportional changes in the thermophysical properties) proceeds at the rate that is determined by the local interface velocity; the phase identifier function keeps track of this conversion process. For those nodes that do not contain the interface, conventional heat flow computation takes place with due consideration given to the absorbed energy (i.e., $S_1$) and the relevant thermophysical properties of the nodes.

Because the interface is conceived as being sharp and computed to be spatially localized within the volume associated with one node, the current approach stands in contrast to the often-utilized equilibrium formulation (i.e., enthalpy method [II.E. 10, 23]). In the latter method, undercooling of the liquid and overheating of the solid are not permitted, and the solid-liquid interface is permitted to be--and can be--delocalized over many nodes; in such a method, the enthalpy profile defines the location, evolution, and kinetics of the interface. The present approach, on the other hand, iteratively treats and keeps track not only of the thermal field but also of the phase domains within each computational step at the interface-containing nodes via the phase-identifier function (which keeps track of the conversion of the phases), the latent heat function (which takes care of the generation or consumption of the latent heat of transformation within the interface containing nodes), and the interface response function (which defines the interface velocity). Such an approach was taken previously in the *one-dimensional* model that was developed for analyzing pulsed laser melting and solidification of Si surfaces [II.E. 12,13]; the current model represents -- to our knowledge -- the first two-dimensional model that implements such a nonequilibrium formulation. (Additional details of the model can be found in reference [II.E. 24] and further discussion will be provided in a future publication).

**SIMULATION RESULTS**

In order to simplify the situation, we have carried out simulations corresponding to melting and solidification of thin crystal Si films. Simulations were carried out at various energy densities, using a square beam profile whose beam width is fixed at 2 μm. A vertical distance between nodes of 20 nm was used for the Si film. A linearized interface response function with a proportionality constant of 6.7 cm/Ks was utilized. A grid of 250 by 5 nodes was employed for representing the Si film, and one of 250 by 15 nodes was employed for representing the substrate. A variable node scheme was implemented in order to reduce the total computation time without sacrificing the accuracy of the results. The sample configuration consisted of a 1,000-Å-thick polycrystalline Si film on an $SiO_2$ substrate. The necessary temperature-dependent thermophysical values were gathered from a number of available sources (see Ref. 14).

The simulation results reveal that there are, as shown in Figs. II.E.2 and 3, two distinct types of solidification behavior that are observed

depending on the energy density of the incident beam. Figures II.E.2a and 2b show the evolution of the solid-liquid interface during melting and solidification, respectively, when the film is irradiated at 500 $mJ/cm^2$. The results are typical of low-energy-density beam-induced melting and solidification and can be characterized as essentially being vertical and one-dimensional. It is only near the edges of the irradiated portion where the two-dimensional aspect of heat flow and phase transformation are manifested. This scenario is obtained for all irradiation conditions that lead to partial melting of the film. Typical vertical regrowth velocities correspond to approximately 2 m/s.

Figures II.E.3a and 3b on the other hand, show the evolution of the solid-liquid interface during melting and solidification when the film is irradiated at a higher energy density of 800 $mJ/cm^2$. Here, the evolution of the interface can be described as being mainly vertical during the melt-in period, but is clearly *lateral* during solidification. This scenario is obtained for those irradiation conditions that lead to complete melting of the irradiated portion of the film. (The exact width of the completely melted region (1) is greater at the top surface of the film than at the oxide interface and (2) can be smaller or larger than the width of the beam depending on the energy density.) Typical lateral regrowth velocities of approximately 10 m/s are obtained. Fig. II.E.4 shows the lateral temperature profile of the nodes corresponding to the bottom portion of the Si film during lateral solidification.

The most directly comparable experimental example corresponds to the projection-irradiation scheme -- as for example implemented in sequential lateral solidification (SLS) of Si films [II.E. 20, 21] -- in which a uniform incident beam is spatially patterned by going through a mask before being incident on a film. The SLS method represents one way of artificially inducing and intentionally controlling the super lateral growth (SLG) phenomenon encountered in single-pulse irradiation of a-Si or small-grained polycrystalline Si films [II.E. 2]. The SLG phenomenon is also intimately related to grain-boundary-localized complete melting and two-dimensional solidification of Si films (which is suggested as a model for the multiple-pulse-induced grain growth observed in irradiation of polycrystalline Si films [II.E. 3]) in that they both correspond to near-complete melting phenomena.

The general shape of the lateral temperature profile shown in Fig. II.E.4 matches the lateral temperature profile predicted previously in the course of analyzing the SLG phenomenon [II.E. 2]. The origin of this thermal contour was identified and attributed to (1) the localized release of the heat of fusion that occurs at the interface during the growth process, and (2) the significant lateral and vertical heat loss that occurs on *both* sides of the interface. The three physical variables that were previously identified as being transient and important in determining the extent to which the lateral growth can proceed -- the interface temperature as a function of time, the bulk liquid temperature as a function of time, and the characteristic length associated with interfacial recalescence as a function of time -- can all be extracted from the simulation results.

One of the definitive conclusions that can be drawn from the quantitative results presented in this paper is that the solidification

velocities that are observed during lateral growth are significantly higher than those observed during vertical regrowth. This outcome simply reflects the deeper interfacial undercooling attained during lateral solidification of thin films that occurs as a direct consequence of the far more efficient two-dimensional removal of the smaller total amount of heat of transformation generated per solidification distance -- due to the thin-film configuration -- at the solidifying interface.

It is important to note that this observation points out the fallacy associated with an often-invoked argument which advocates that a slower solidification rate leads to a larger grain sized polycrystalline material [II.E. 6-8]. If this were in fact the case, one would expect to obtain polycrystalline Si films with smaller grains for those conditions that lead to lateral solidification; experimental results clearly indicate otherwise [II.E. 18-21]. In the absence of any nucleation of solids in a supercooled liquid, the evolution of the microstructure during epitaxial regrowth of an elemental system is determined mainly by (1) the microstructure of the unmelted portion of the material in contact with the liquid at the start of solidification and (2) the occlusion among growing grains that occurs during the ensuing solidification. (Fracturing of dendrites [II.E. 25] and breakdown of epitaxial growth are two other means through which the microstructure can be affected). These principles, when viewed together with the current results (which indicate that significantly greater solidification distances are attained during lateral growth) explains -- and is consistent with -- the experimentally obtained microstructures wherein significantly larger and elongated grains are observed for all those conditions that induce substantial lateral solidification of Si films [II.E. 18].

In summary, we have used a newly developed transient two-dimensional model to simulate localized excimer-laser beam-induced melting and solidification of thin silicon films on $SiO_2$. The results reveal -- and describe in quantitative detail -- two distinct types of solidification behavior as a function of incident energy density: at low energy densities, partial melting and predominantly vertical solidification occurs within the irradiated area, while at high energy densities, complete melting of a portion of the film is followed by rapid lateral solidification. These results are entirely consistent with the transformation scenarios deduced from experimental observations.

## II.E. SEQUENTIAL LATERAL SOLIDIFICATION OF THIN SILICON FILMS

### II.E1: GENERAL ASPECTS OF SLS AND USE OF THE SLS PROCESS FOR PRODUCING A DIRECTIONALLY SOLIDIFIED MICROSTRUCTURE

#### SECTION SUMMARY

Sequential lateral solidification is a low-temperature excimer-laser-crystallization process that produces a previously unattainable directionally solidified microstructure in thin Si films. The process involves (1) inducing complete melting of selected regions of the film via projection-irradiation through a patterned mask, and (2) precisely controlled between-pulse microtranslation of the sample with respect to the mask over a distance shorter than the single-pulse lateral solidification distance, so that lateral growth can be extended over a number of iterative steps. We demonstrate how the SLS process can be easily extended to produce large single-crystal regions on glass substrates.

#### TECHNICAL MOTIVATION FOR THE SLS PROCESS

Thin-film-transistor (TFT) devices fabricated from Si films on $SiO_2$ can perform in a number of applications for which conventional monolithic-Si-wafer-based devices are ill-suited. Currently, much interest and effort are being focused on developing high-quality TFTs for *integrated* active-matrix liquid-crystal displays (IAMLCDs) and static random-access-memory (SRAM) devices.[1,2] Three-dimensional integrated circuits represent a less well recognized, but potentially significant future TFT application.

Previous investigations have revealed that in order to achieve the requisite level of TFT performance at which these applications can be effectively addressed, it is necessary to fabricate the devices on crystalline Si films.[3] While the technology for producing TFT devices from hydrogenated thin amorphous Si films already exists, and amorphous-Si-based TFTs are implemented on a routine basis as pixel-controlling transistors in the production of AMLCDs, these devices have intrinsic performance limitations that make them inadequate for more demanding applications. Furthermore, the process by which the crystalline Si films are produced must not involve high temperatures, so as to be compatible with low-cost glass substrates in the case of production of IAMLCDs, and to prevent the degradation of the underlying devices in the case of production of three-dimensional integrated circuits. For this and additional reasons,[4] the nearly perfect single-crystal Si films that can be prepared via conventional silicon-on-insulator (SOI) or SOI-derived processes are not fully appropriate for these applications.

In response to such well-defined technological needs, a number of solid-phase and excimer-laser crystallization (ELC) techniques that convert an as-deposited amorphous Si film into a crystalline Si film have been investigated in recent years.[4-6] The end products of these processes range from small-grained to large-grained polycrystalline Si films that unfortunately and invariably contain randomly located grain boundaries

throughout the crystallized area. This being so, the performance of devices that are built on these materials is inevitably lacking; the preponderance of grain boundaries in small-grained Si films leads to poor device characteristics on one hand, and the inherent randomness of the microstructure in large-grained Si films leads to poor device uniformity on the other.[5]

Here, we elaborate on a new excimer-laser crystallization process endowed with a previously unavailable combination of features that make it capable of tackling various TFT applications in an effective manner. The process, which we call sequential lateral solidification (SLS), is compatible with low-temperature substrates, and *yet* produces a directionally solidified microstructure that consists of nonequiaxed grains of unrestricted length; such a microstructure makes the SLS-processed Si films the best low-temperature-substrate-compatible TFT material that has been obtained to-date. More significant is the fact that the SLS process can be used for directly producing the ideal material for fabricating the highest quality TFT devices: large, location-controlled single-crystal Si regions (i.e., areas that are completely free of grain boundaries) on top of substrates that are intolerant of high processing temperatures.

**BASIC SLS PROCEDURES**

The SLS process entails projection-irradiation of an Si film through a patterned mask, and precise between-pulse microtranslation of the film with respect to the mask. The experimental details are as follows: The crystallization apparatus consisted of an excimer laser operating at 308 nm (XeCl) and with a pulse duration of 30 ns, a UV projection system, a patterned mask, and a sub-micrometer-precision translation stage. A schematic diagram of the apparatus is shown in Fig. II.F1.1. The projection system included a variable-energy attenuator, a variable-focus field lens, and a two-element imaging lens. The UV mask used in these experiments was fabricated on a molybdenum silicide coated quartz plate, and the pattern consisted either of an array of narrow parallel slits such that only the portion of the original beam that passed through the slits was transmitted. The relative positions of the mask, imaging lens, and sample were adjusted to yield a pattern demagnification ratio of approximately 5X. At this demagnification, the image of each slit had a width of 5 μm at the sample plane. The samples consisted of oxidized (100) Si substrates with a 1.9-μm-thick $SiO_2$ isolation layer, on top of which 2,400-Å-thick a-Si films were deposited via LPCVD.

The crystallization procedure consisted of repeatedly irradiating the sample at an energy density sufficient to induce complete melting of the exposed (non-masked) areas of the film. Concurrently, the sample was translated in a direction perpendicular to the long axis of the projected image of the mask slits. The laser pulse frequency was 1 Hz, and the stage translation rate was 0.75 μm/s, resulting in a per-pulse translation distance of 0.75 μm. All experiments were conducted under ambient conditions, and with the samples at room temperature. After irradiation, some samples were defect-etched (Secco-etchant) and examined via optical microscopy and SEM, while others were prepared for TEM observation via a back-etch technique.

**EXPERIMENTAL OUTCOME:**

Fig. II.F1.2(a) is a low-magnification optical micrograph of an SLS-processed and defect-etched Si film. The film contains a number of location-controlled irradiated zones in the form of "squares". All of these squares were irradiated simultaneously, and each one corresponds to the area scanned by an individual slit of the mask pattern. Close inspection of the microstructure within each square reveals it to consist of directionally solidified grains, which contain low-angle intragrain sub-boundaries, that form a lineage (or "river"-like) pattern[7] and which, if not occluded along the way by competing adjacent grains, extend throughout the entire translation distance of 200 μm (i.e., the size of the non-occluded grains is equal to the total translation distance). Higher magnification shows more clearly the extremely long directionally solidified grains separated by nearly parallel grain boundaries, as can be seen in Figs. II.F1.2(b) and 3, which are SEM and TEM micrographs, respectively, of an SLS-processed film. The grain boundaries and sub-boundaries tend to be aligned, and lie approximately parallel to the growth direction (i.e., perpendicular to the melt interface at any given time). The competition between adjacent growing grains often leads to occlusion of those grains that are less favorably oriented to grow, as can be seen in Figs. II.F1.2(b) and 3--especially in Fig. II.F1.3(a), which shows the region where directional lateral solidification initiated. Because of this competition, only a fraction of the grains that are originally present at the start of growth survive to the end of the translation, and the average width of the grains increases with increasing translation distance.

The SLS process derives from previous investigations in which we identified and described the various melt-mediated crystallization scenarios that are manifested in ELC of amorphous Si films on $SiO_2$.[8] It is one of several such processes that are currently under development; these techniques are collectively referred to as the artificially controlled super-lateral growth (ACSLG) method in that they essentially amount to artificially inducing and precisely manipulating the super-lateral growth (SLG) phenomenon.[9] A theoretical description of the process has been provided previously,[9] and a quantitative analysis of the process has recently been accomplished using a newly developed two-dimensional numerical model.[12] Further discussion of the factors involved in the ACSLG process can also be found in References 10 and 11.

The following is a description of the basic features of the working model of the SLS process: In SLS, complete melting of selected areas--and subsequent lateral solidification--is induced via projection irradiation of the film (i.e., complete melting occurs in those areas that are irradiated through the patterned mask). Lateral growth from the masked regions proceeds into the molten region as the film cools. Then, the sample is translated with respect to the image of the mask aperture over a distance less than the single-pulse lateral-growth distance, and is irradiated again. Once more, this results in complete melting of the exposed areas. Lateral growth recommences from the edge of the completely molten region, which is now located within--as far as the solidification front is concerned--the laterally grown grains produced during the previous irradiation. In this manner, *lateral*

*growth of the grains can be continued over each iterative step, resulting in grains much longer than the single-pulse-induced lateral-growth distance.* Since the process can be repeated indefinitely, arbitrarily long grains can be produced. (A more detailed description requires an involved analysis of melting and solidification, and is planned for a future publication.)

The foregoing analysis of the SLS process dictates that in order to successfully carry out the process, it is necessary (1) that the irradiation energy density be sufficiently high to induce complete melting in the exposed areas, and (2) concomitantly that the per-pulse translation distance be less than the single-pulse lateral-growth distance. It follows that the energy-density processing window is bounded at the lower end by the energy density that is needed to completely melt the exposed portion of the film. At the other extreme, excessive irradiation of the film can lead to agglomeration, whereby the molten region of the film beads up and leaves the underlying $SiO_2$ exposed.[13]

The line-beamlet-processed SLS microstructure, with its long, parallel grains and extensive branched network of subboundaries, bears a resemblance to the microstructures obtained in zone-melting recrystallization (ZMR) of thin Si films--one of the conventional SOI methods. This resemblance is not surprising since both processes utilize an energy beam to induce localized melting and subsequent lateral solidification of Si films in order to obtain directionally grown crystals. Fundamentally, there is a major difference between the two methods as ZMR is a steady-state near-equilibrium process whereas SLS is an ultrarapid far-from-equilibrium process. This difference makes SLS applicable to low-temperature glass substrates, while the ZMR process must utilize Si wafers or quartz substrates. The distinguishing features of the SLS process include (1) its compatibility with low-temperature processing requirements, (2) the capability to process very thin Si films, and (3) the ability to process a large number of areas simultaneously. Additionally, the SLS process avoids the wafer wDARPAge, impurity contamination, and Si-substrate-melting problems that are often encountered in the ZMR method.[13]

As stated earlier, most of the defects appear to be low-angle subboundaries. This observation has an important ramification for performance of TFT devices fabricated on these materials: In contrast to high-angle grain boundaries, which are profoundly detrimental to majority-carrier-based devices, the subboundaries, as they consist of isolated dislocations,[14] are considered to be benign as regards the performance of TFTs.

SECTION II.E2 SINGLE-CRYSTAL Si FILMS FOR THIN-FILM TRANSISTOR DEVICES VIA SLS USING CHEVRON-SHAPED BEAMLETS

**SECTION II.E2 SUMMARY**

The fact that single crystal Si would make an ideal material for thin-film transistor devices has long been recognized. Despite this awareness, a viable method by which such a material could be directly produced on a glass substrate has never been formulated. Here, we show experimentally that location-controlled single-crystal Si regions on an $SiO_2$ surface can be obtained via excimer-laser-based sequential lateral solidification of thin Si films using a beamlet shape that self-selects and extends a single grain over an arbitrarily large area. This is accomplished by controlling the locations, shape, and extent of melting induced by the incident excimer-laser pulses, in such a manner as to induce interface-contour-affected sequential super-lateral growth of crystals, during which the tendency of grain boundaries to align approximately orthogonal to the solidifying interface is systematically exploited.

**MOTIVATION FOR SINGLE-CRYSTAL Si FILMS**

Silicon-based thin-film transistors (TFTs) fabricated on glass substrates have emerged in recent years as an important, distinct, and actively pursued category of microelectronic devices [II.F2. 1]. As expected from device physics considerations, the phase and microstructure of the Si film on which the devices are fabricated determine the performance characteristics and device-to-device uniformity of the resulting TFTs [II.F2. 2, 3]. Unfortunately, existing Si preparation methods produce amorphous, microcrystalline, or polycrystalline Si films that invariably contain intrinsic microstructural deficiencies that lead to corresponding shortcomings and limitations in the resulting TFTs.

The most direct and effective solution that will eliminate the above microstructural problem, and which can enable a number of immediate and timely improvements as regards nearly all aspects of device performance, has been apparent but previously out of reach: synthesize and utilize single-crystal Si films on glass substrates [II.F2. 4]. The reasons behind the difficulties that are encountered in attempting to do so can be readily traced to two unyielding characteristics of glass substrates: Primarily, the amorphous nature of glass makes it impossible to employ a number of existing vapor-, liquid-, and solid-phase epitaxial growth/regrowth processes that take advantage of the crystalline character of the substrates [II.F2. 5, 6, 7, 8]. Secondly, the inability of glass to withstand sustained processing at high temperatures makes it unpractical to utilize the steady-state directional solidification processes previously developed for producing single-crystal Si films (i.e., zone-melting recrystallization of Si films on $SiO_2$ using a cw laser, a focused lamp, an electron-beam, or a graphite-strip heater [II.F2. 9]).

Here, we summarize a glass- (or plastic-) substrate-compatible method by which low-defect-density single-crystal Si films can be realized. Specifically, our excimer-laser-based sequential lateral solidification

(SLS) method leads to formation of location- and dimension-controlled single-crystal regions on an $SiO_2$ surface. The short pulse duration of an excimer-laser beam prevents sustained heating of the underlying substrate, and makes the process compatible with glass substrates [II.F2. 1, 4].

**EXPERIMENTAL PROCEDURES**

The samples consisted of Si substrates with a 1.9-μm-thick $SiO_2$ isolation layer, on top of which 2,000-Å-thick a-Si films were deposited via LPCVD using silane gas at a deposition temperature of 580 °C. The thickness of the oxide layer was chosen to be sufficiently thick so as to thermally isolate the underlying Si substrate. The experimental apparatus consisted of an excimer laser operating at 308 nm (XeCl), a UV projection system, and a sub-micrometer-precision translation stage. The UV mask used in these experiments was fabricated out of molybdenum silicide on a quartz substrate, and the pattern consisted of an array of chevron-shaped apertures on an opaque background such that only the laser radiation that passed through the narrow slits was transmitted. At the 5X demagnification used, the image of each chevron had a slit width of 5 μm at the sample plane, and was 50 μm across.

Processing was carried out by iteratively (1) irradiating the sample at an energy density sufficient to induce complete melting of the silicon film in the exposed areas (approximately 900 $mJ/cm^2$ for the 2,000-Å thickness), and (2) translating relative to the beam over a distance (typically 0.75 μm) approximately one-half of the single-pulse lateral growth distance. This process was repeated over a total translation distance of 50 μm. The majority of the samples were Secco-etched and examined via optical microscopy; others were prepared for transmission electron microscopy (TEM) observation via a back-etch technique.

**DESCRIPTION OF RESULTS**

Figure II.F2.1(a) is a low-magnification optical micrograph of a defect-etched SLS-processed sample that shows a bird's eye view of the irradiated area. All of the regions were processed simultaneously, and each individual crystallized region represents the area processed by a single chevron feature on the mask. Figure II.F2.1(b) is a higher magnification optical micrograph that shows a defect-etched region crystallized by a single chevron, and Figure II.F2.1(c) is the corresponding darkfield image. The dashed lines in Fig. II.F2.1(b) delineate the boundaries between the single-crystal region (I) and regions II, which have a lateral columnar microstructure identical to that observed in previous SLS experiments conducted using a mask consisting of straight slits [II.F2. 10]. Figure II.F2.2 is a planar view TEM micrograph of a crystallized film. Figure II.F2.2(a) shows, among other things, that a narrow polycrystalline transition border lies between the interior of the crystallized area (i.e., regions I and II) and the outer amorphous matrix area.

The most striking feature within region I corresponds to a nearly perfect and defect-free central portion that is bordered on each side by regions with a number of linear defects [see Figs. II.F2.1(b,c) and 2]. These defects correspond to lineage boundaries in that they terminate in the interior of the single-crystal region; that is, it is possible to go

from any point in a lineage structure to any other point without crossing a boundary. They therefore cannot be high-angle grain boundaries, but must instead correspond to sub-boundaries. This observation, in turn, qualifies the whole of region I as being single-crystal material, albeit containing sub-boundaries. Note that (1) the size of the single-crystal region is determined by, and can be controlled simply by varying the width of the beamlet incident on the sample surface and the total translation distance, and (2) the number and location of these regions can be precisely controlled by using an appropriately patterned mask.

Sequential lateral solidification is one of the artificially controlled super-lateral growth (ACSLG) techniques [II.F2. 4, 10, 11, 12] that were formulated based on the transformation- and microstructure-related insights previously obtained from a set of investigations in which we identified and categorized a number of far-from-equilibrium solidification scenarios that can occur when a thin Si film on oxide is irradiated with an excimer laser [II.F2. 13, 14, 15, 16]. In particular, the super-lateral growth (SLG) phenomenon, which was identified [II.F2. 13] and subsequently analyzed [II.F2. 14], formed the template for these ACSLG processes in that the processes all take advantage of the lateral growth of solids that results when a completely molten region is in contact with an incompletely molten portion of a film at the maximum point of melting. *The limited extent to which the lateral growth can proceed following a single pulse is determined by several thermal and kinetic factors, and is ultimately constrained by the eventual nucleation of solids in a supercooled liquid* [II.F2. 14].

As described in the previous section, the SLS process overcomes this lateral growth limitation via an iterative irradiation scheme that involves precisely coordinated between-pulse translation of the film with respect to the beamlets such that it becomes possible to continue the epitaxial lateral growth of the grains. The end result is that despite the rapid, transient, and far-from-equilibrium nature of excimer-laser-induced solidification (which is responsible for making this high-temperature process compatible with glass substrates), it can produce microstructures that are equivalent to those that are obtained via slow, steady-state, near-equilibrium directional solidification processes [II.F2. 9]. The excimer-laser projection-irradiation scheme represents one of several possible ways of carrying out the SLS process; alternative pulsed-energy sources and various beam-shaping methods can be used for carrying out SLS.

In general, the development of the microstructure of an elemental system during epitaxial solidification with a planar interface is governed primarily by (1) the microstructure of the unmelted portion of the material in contact with the liquid at the start of solidification, and (2) the occlusion among directionally growing grains. Implicit in the previous statement--and a point that is often taken for granted in discussing microstructural development during solidification, and which has been exploited in a number of solidification processes [II.F2. 9, 17]--is the fact that during solidification, the grain boundaries (as well as dislocations and sub-boundaries) tend to orient themselves approximately normal to the advancing planar solid-liquid interface

[II.F2. 17]. This interface-microstructure correlation is what is being exploited in the current work.

Viewed from this perspective, the skewed melt front relative to the translation direction of the beam forces the grain boundaries on either side of a chevron to be effectively and gradually pushed out to the respective edges of the chevron and terminated. This in turn means that the single grain that is fortuitously located at the tip of the chevron will initially expand in both directions, and eventually dominate the growth over the entire region, as for example observed in Figures II.F2.1(b,c) and 2(a), and schematically illustrated in Figure II.F2.3. The exact details of the grain boundary evolution in the initial phase of the process, during which the grain establishes dominance over the central portion, further involves consideration of (1) the curvature of the solid-liquid interface, which tends to be smoothed out by a number of factors including defocusing, interference effects, thermal diffusion, and solid-liquid interface tension; (2) the density of the grains at the initiating polycrystalline Si-liquid interface; and (3) the competitive occlusion of the grains.

The small- and fine-grained polycrystalline transition region on the periphery of the irradiated area, on the other hand, originates from vertical and lateral explosive crystallization, as well as solidification following partial melting and near-complete melting of the film [II.F2. 13].

The presence of sub-boundaries within the single-crystal region is not unexpected; they were previously identified as one of the major defects observed in SLS-processed Si films, and were also prevalent in zone-melting recrystallized Si films [II.F2. 9]. They form by the coalescence of dislocations, which can be generated as a consequence of a number of different causes [II.F2. 17, 18]. What is unexpected and fortuitous is the absence of sub-boundaries and other types of TEM-observable defects within the central portion of the single-crystal region [see Fig. II.F2.2(b)]. The near silicon-on-insulator (SOI) quality of the region makes it an ideal location on which to strategically place the active-channel portion of a device. This can be accomplished because the nearly defect-free region is predictably and precisely located at the central portion of the crystallized area, and the width of the region appears (based on the experiments conducted to date) sufficiently wide (typically $\geq$ 10 μm) for placing the active-channel region of typical TFT devices.

**IMPLICATIONS OF THE MATERIAL/METHOD**

At the very least, the method presented herein represents the first viable procedure for directly obtaining single-crystal Si films on any $SiO_2$ coated substrates, including those that cannot withstand sustained processing at high temperatures, such as glass and plastics. As such, the idea of fabricating low-temperature single-crystal Si TFT (LT s-Si TFT) devices on such substrates can now be put into practice.

At most, the method stands to address any applications that can benefit from the availability of single-crystal Si on an arbitrary substrate. Presently, integrated active-matrix liquid-crystal displays (IAMLCDs) are the most actively pursued application [II.F2. 4]. Here, the SLS

process can provide the means for manufacturing highly integrated IAMLCDs and should eventually make it feasible to develop "system-on-glass" products [II.F2. 4].

In addition to integrated AMLCDs, the unique combination of the SLS process and material may be applicable to a number of other large-area electronics and Si-integrated-circuit applications including three-dimensional integrated circuits, megabit static random-access memory (SRAM), integrated active-matrix electroluminescent displays, image (and other) sensors, certain SOI applications, and crystalline-Si-based thin-film solar cells. It is also conceivable that some integrated circuits that are currently fabricated using conventional single-crystal wafer technology may in the future be manufactured on alternative substrates using the SLS process.

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**Figure Captions - SECTION II.A.**

Table 1. Various melt-meditated transformation mechanisms observed in single-pulse-induced crystallization of LPCVD a-Si films on $SiO_2$ (from Ref. II.A.53).

Figure 1. Schematic representation of the top view of TFT devices fabricated on films with various microstructures: (a) and (b) correspond to small-grained and random large-grained poly-Si, respectively, and represent currently available technology; (c) corresponds to grain-boundary-location-controlled poly-Si; and (d) corresponds to single-crystal Si -- the ultimate microstructure for TFT devices.

Figure 2. Planar-view bright-field TEM images of single-pulse-crystallized LPCVD Si films at various energy densities. The first sequence (a-e) and the second sequence (f-j) correspond to oxide-capped samples irradiated with the substrates at room temperature and 550 °C, respectively. The irradiation energy densities were as follows: (a) 125, (b) 135, (c) 200, (d) 230, (e) 280, (f) 76, (g) 120, (h) 145, (i) 170, and (j) 245 $mJ/cm^2$ (from Ref. II.A.53).

**Figure Captions - SECTION II.C.**

Figure 1. Planar-view bright-field TEM images of single-pulse-irradiated 1000-Å-thick Si films with oxide stripes on top (2-μm-wide/1.5-μm-separated) at various energy densities (all at the substrate temperature of 150 °C) (a) 190 $mJ/cm^2$, (b) 290 $mJ/cm^2$, (c) 340 $mJ/cm^2$, and (d) 385 $mJ/cm^2$.

Figure 2. Planar-view bright-field TEM images of single-pulse-irradiated 2400-Å-thick Si films (with 10-μm-wide/1.5-μm-separated oxide stripes on top) at substrate temperatures of (a) 400 °C and (a) 700 °C, at energy densities of (a) 435 $mJ/cm^2$ and (c) 265 $mJ/cm^2$. (The detailed explanation for the various microstructural features which are observed in the above micrographs is found in Ref. II.C.5.)

Figure 3. Variations in (a) the linear density of grain boundaries (i.e., the number of grain boundaries encountered per 10 μm, in the direction parallel to the stripes) and (b) the fraction of grains which continuously grew and extend (i.e., not occluded) to the center of the GLC region as a function of the distance from the center of the GLC area for 2400-Å-thick Si films with 10-μm-wide oxide stripes.

Figure 4. Schematic view of the strategically placed TFT devices on the grain-boundary-location-controlled (GLC) Si films such that (a) a single perpendicular grain boundary and (b) zero perpendicular grain boundaries are encountered by the traveling majority carriers within the active-channel regions.

**Figure Captions - SECTION II.D.**

FIG. 1. Planar-view bright-field optical micrographs of islands (a) before irradiation and (b) after irradiation at 1,150 °C.

FIG. 2. Planar-view optical Nomarski micrographs of Secco-etched islands irradiated at (a) 1,150 °C and (b) 1,100 °C.

**Figure Captions - SECTION II.E.**

Figure 1: A schematic of the sample configuration and the lateral beam profile. The pulse duration of the excimer laser is 36 ns.

Figure 2: The location of the solid-liquid interface under laser irradiation of 500 $mJ/cm^2$. Melting sequence is shown in (a) at 15 ns (o), 20 ns (Δ), 30 ns (+), and solidification sequence is shown in at 35 ns (o), 50 ns (Δ), 60 ns (+). Note that the x and y axes have different scales.

Figure 3: The location of the solid-liquid interface under laser irradiation of 800 $mJ/cm^2$. Melting sequence is shown in (a) at 10 ns (o), 15 ns (Δ), 20 ns (+), 30 ns (☆)and solidification sequence is shown in (b) at 35 ns (o), 65 ns (Δ), and 95 ns (+). Note that the x and y axes have different scales.

Figure 4: The temperature profile at 90 ns of the nodes corresponding to the bottom portion of the Si film during lateral solidification.

**Figure Captions - SECTION II.F1.**

FIG. 1. Schematic diagram of an ELC projection system configured for the SLS process.

FIG. 2. (a) Optical and (b) SEM micrographs of defect-etched 2,400-Å-thick silicon films directionally crystallized using the SLS process. The translation rate was 0.75 μm/pulse, over a total translation distance of 200 μm. The arrows show the direction of the sequential lateral growth.

FIG. 3. (a-c) Planar-view bright-field TEM images, at various magnifications and locations, of 2,400-Å-thick silicon films directionally crystallized using the SLS process. The translation rate was 0.75 μm/pulse, over a total translation distance of 200 μm (in the direction from the bottom to the top of the pictures). The region where directional lateral solidification initiated is shown in (a). The bottom portion of the picture shows amorphous silicon, followed by a polycrystalline transition zone, and then the directionally solidified SLS material; (b) and (c) correspond to regions further removed from the initiation point.

**Figure captions - SECTION II.F2.**

FIG. 1. Optical micrographs of a defect-etched SLS-processed film; (a). low magnification. The arrow shows the solidification direction, and the magnitude of translation. (b) high magnification, brightfield, with dotted lines demarcating the boundaries between the single-crystal and columnar crystal regions; (c) high-magnification darkfield.

FIG. 2. Planar-view TEM pictures of SLS-processed films; (a) lower magnification, showing the entire region processed by a single chevron beamlet. The area within the dotted square corresponds to that shown in (b); (b) higher magnification micrograph showing the nearly defect-free central portion.

FIG. 3. Schematic views showing the microstructural development during the initial stages of the SLS process using a chevron-shaped mask pattern; (a) first irradiation pulse through mask, as indicated by the dashed outline; (b) second pulse. These figures show the microstructure that results when the molten region is narrow, and lateral growth is terminated by the two opposing growth fronts colliding at the center. *When the molten zone is sufficiently wide, bulk nucleation of solids inevitably occurs in the middle of the completely molten area* [II.F2. 11].

## Table I: Various Melt-Meditated Transformation Mechanisms Observed in Single- Pulse-Induced Crystallization of Low-Pressure-Chemical-Vapor-Deposited a-Si Films on $SiO_2$.[53]

I. Partial-Melting Regime (Low-Energy-Density Regime)
- Continuous layer of unmelted film at the $SiO_2$ interface (i.e., melt depth< film thickness)
- Explosive crystallization, vertical regrowth (competitive occlusion of grains)
- Fine-grained and small-grained polysilicon (grain radius < film thickness)

II. Near-Complete-Melting Regime (Superlateral-Growth Regime)
- Unmelted Si composed of discrete islands (i.e., melt depth ≈film thickness)
- Significant lateral growth can proceed before impingement
- Up to~ μm-sized grains observed

III. Complete-Melting Regime (High-Energy- Density Regime)
- Deep supercooling followed by nucleation and growth of solids
- For low substrate temperatures (T< 600 °C), fine-grained and small-grained polysilicon observed (grain radius < a few hundred Å)
- Amorphization observed for thinner films

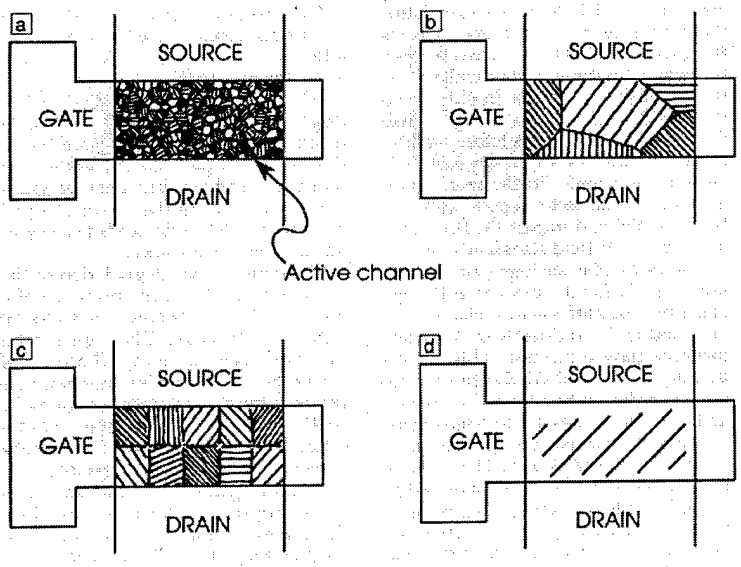


Fig.II.A.1.

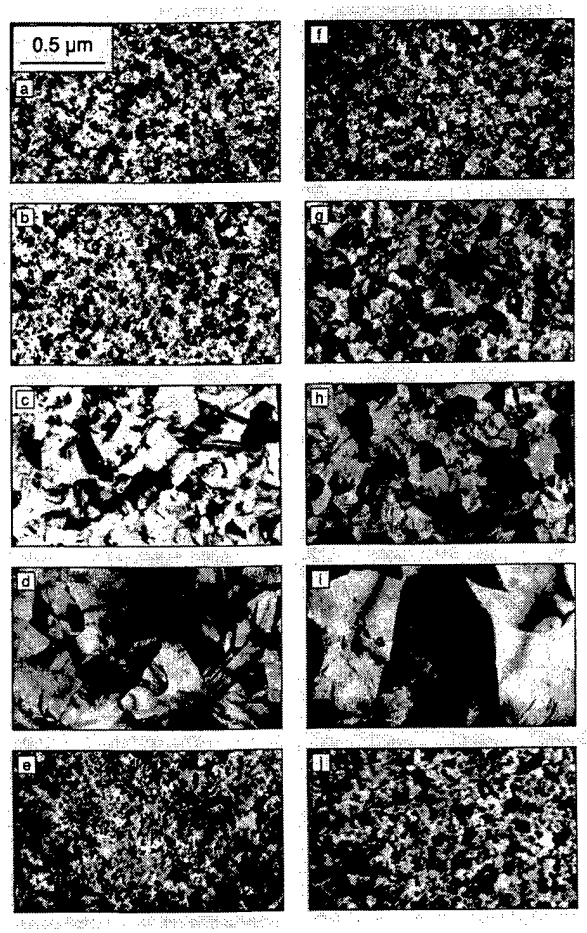


Fig. II.A.2

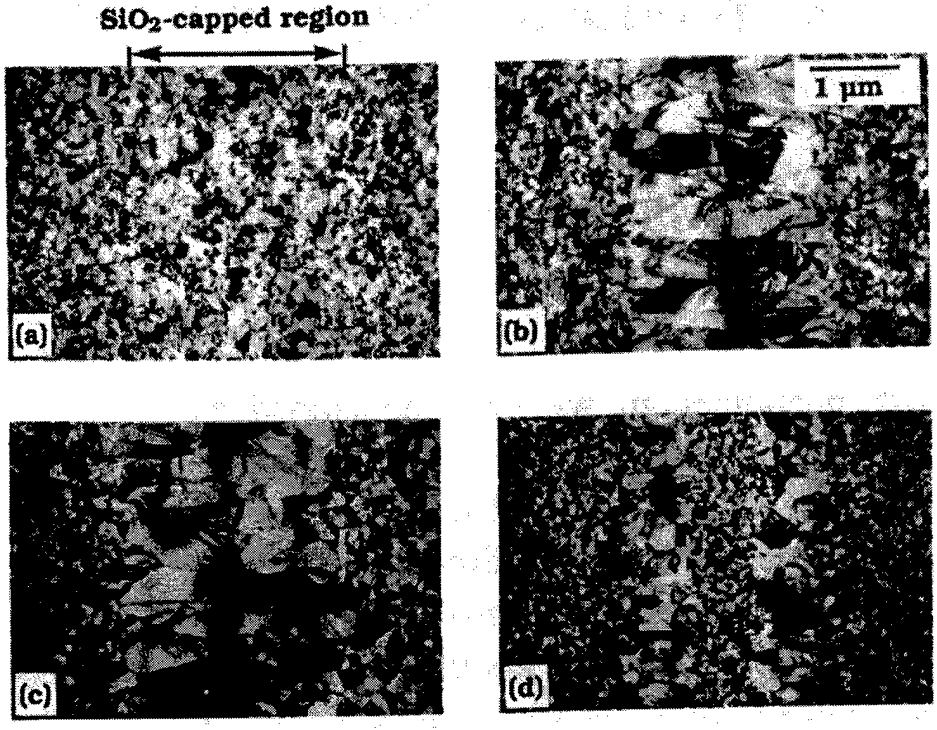


Fig. II.C.1

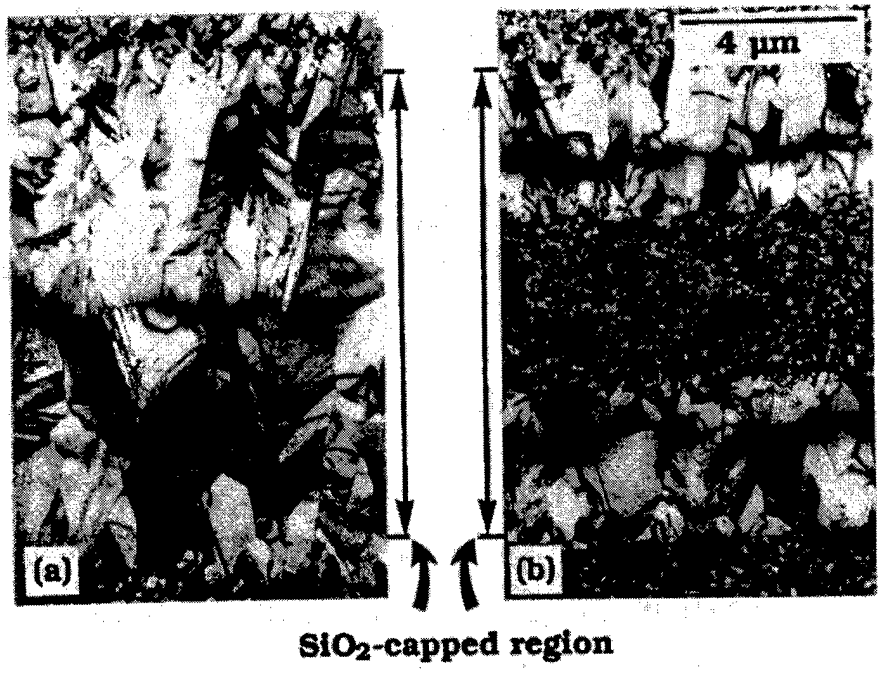


Fig. II.C.2

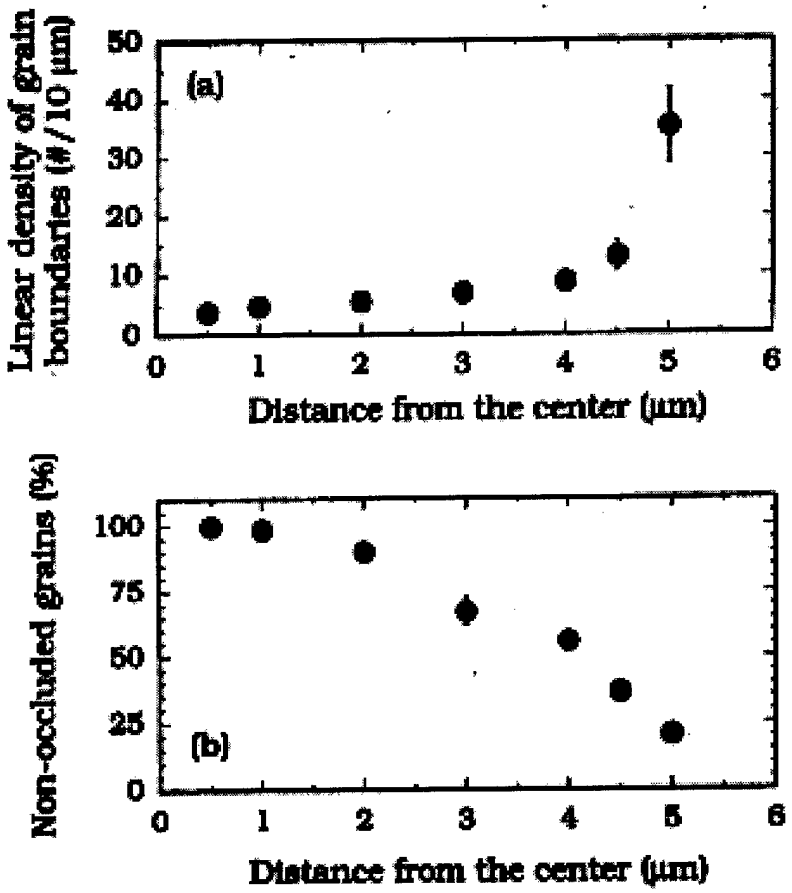


Fig. II.C.3

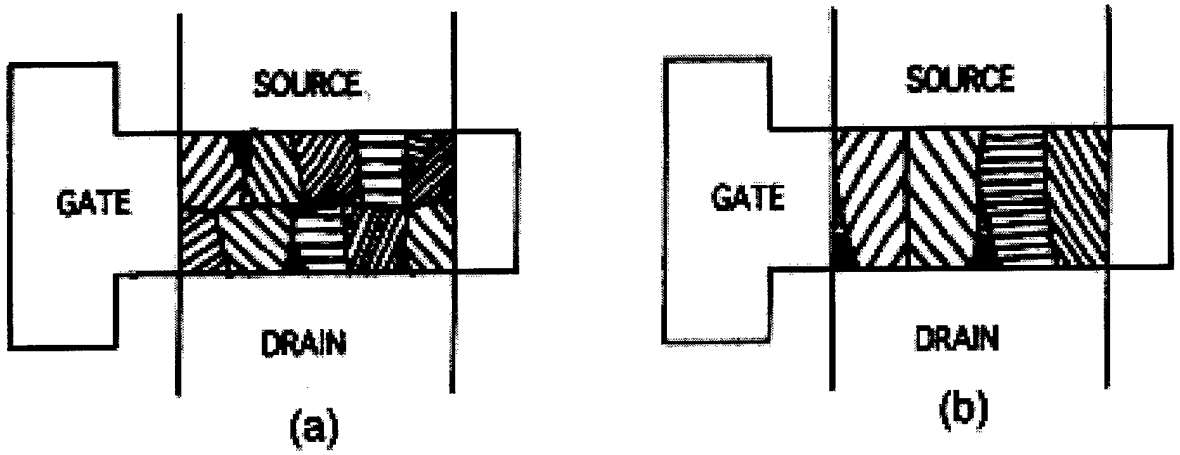


Fig. II.C.4

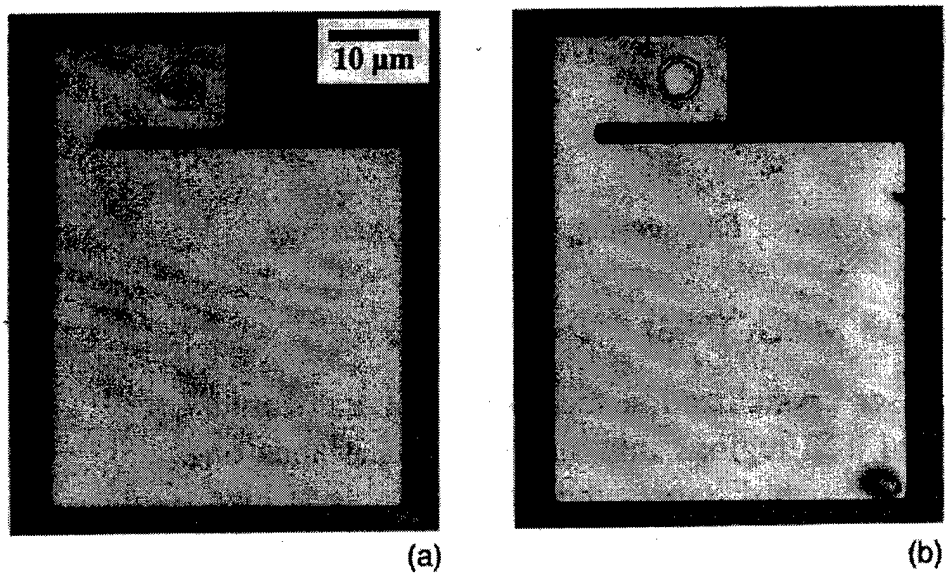


Fig. II.D.1

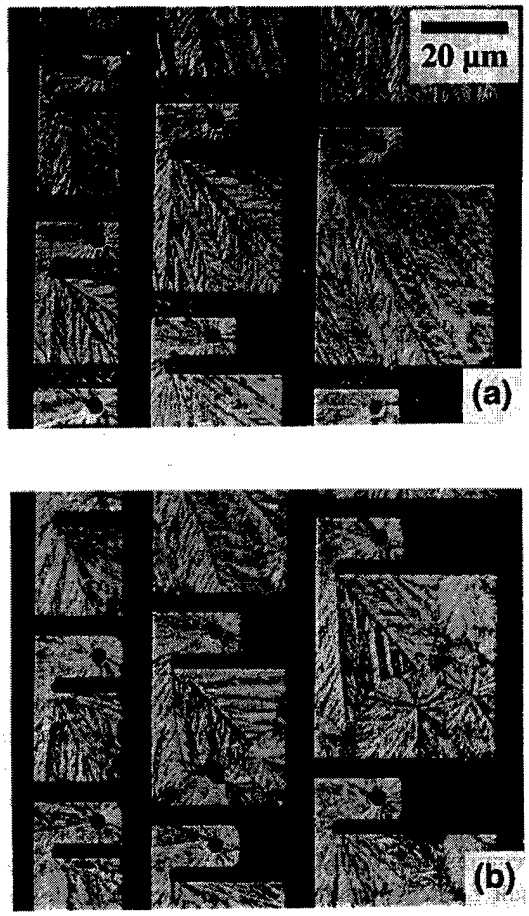


Fig. II.D.2

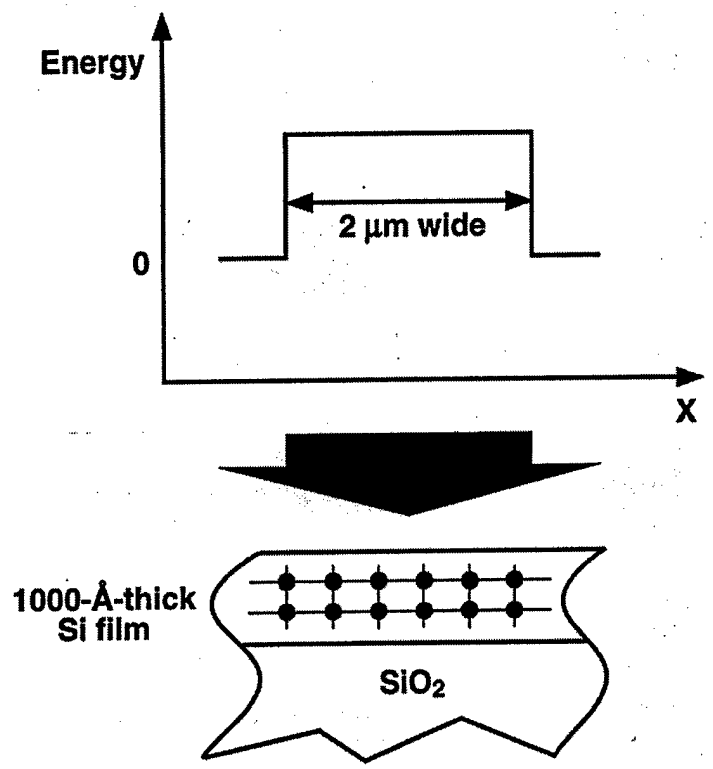


Fig. II.E.1

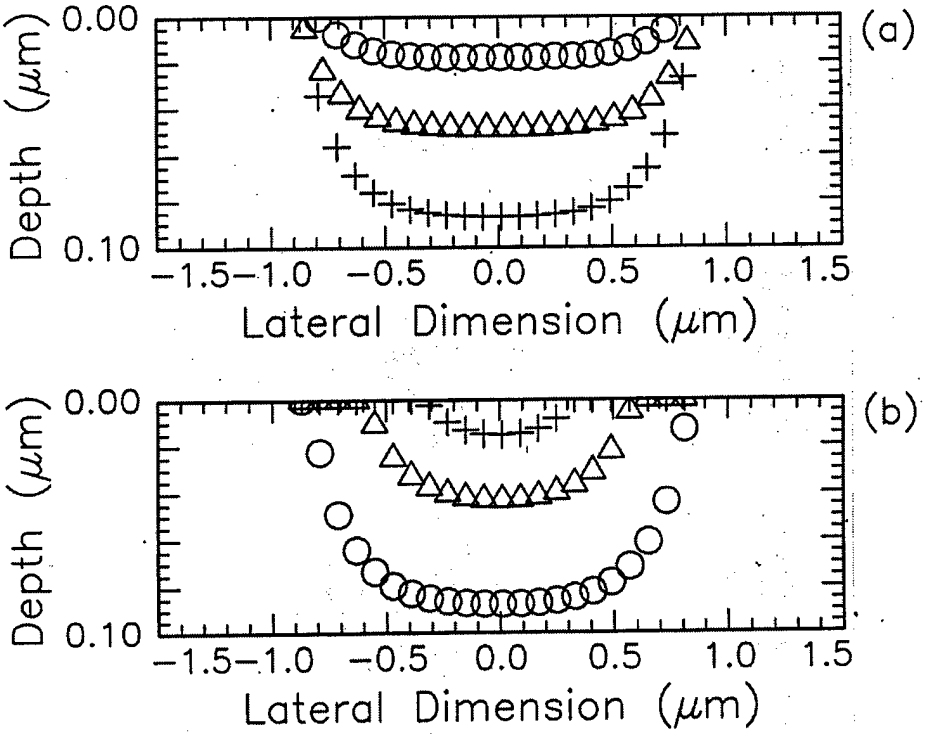


Fig.II.E.2

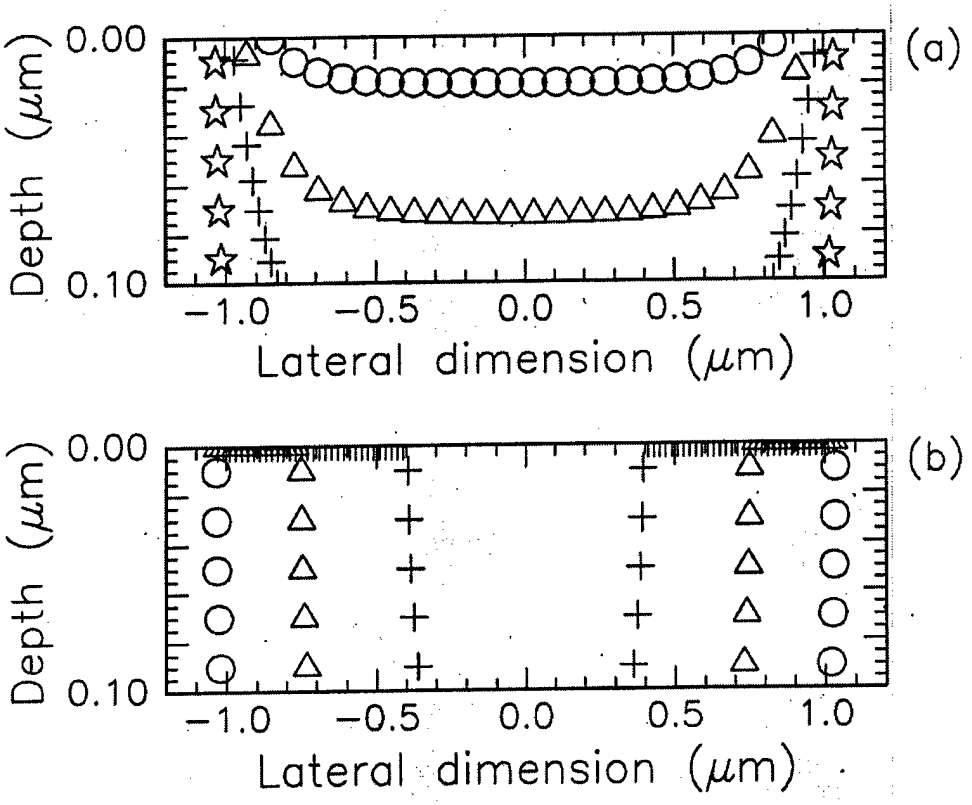


Fig. II.E.3

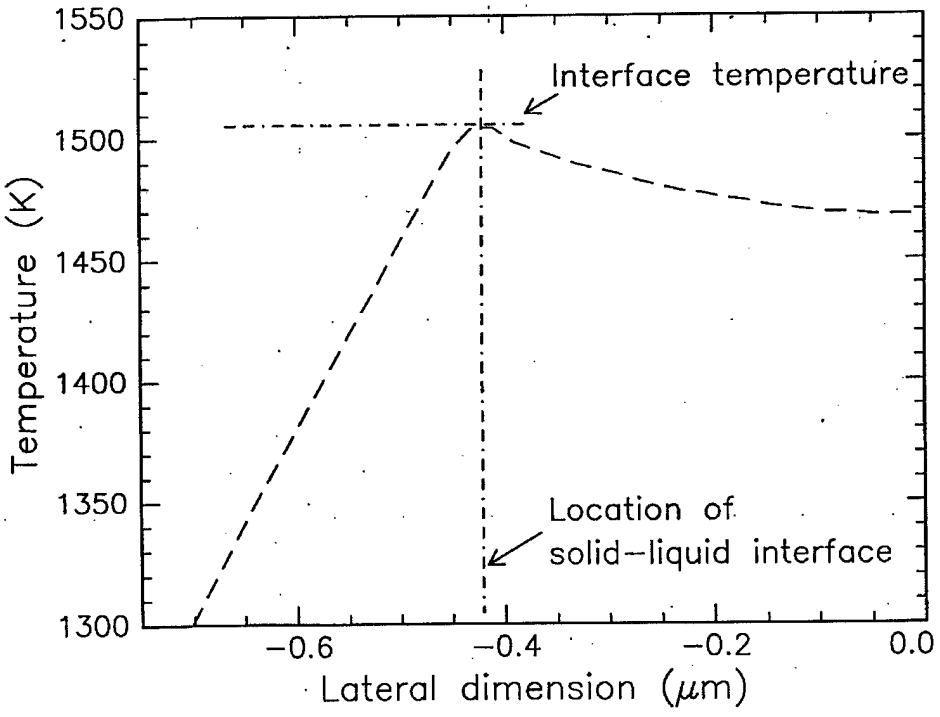


Fig. II.E.4

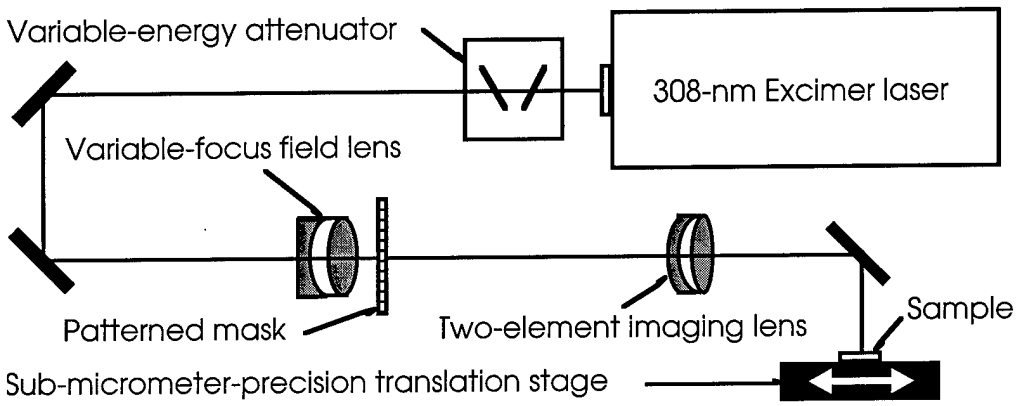


Fig. II.F1.1

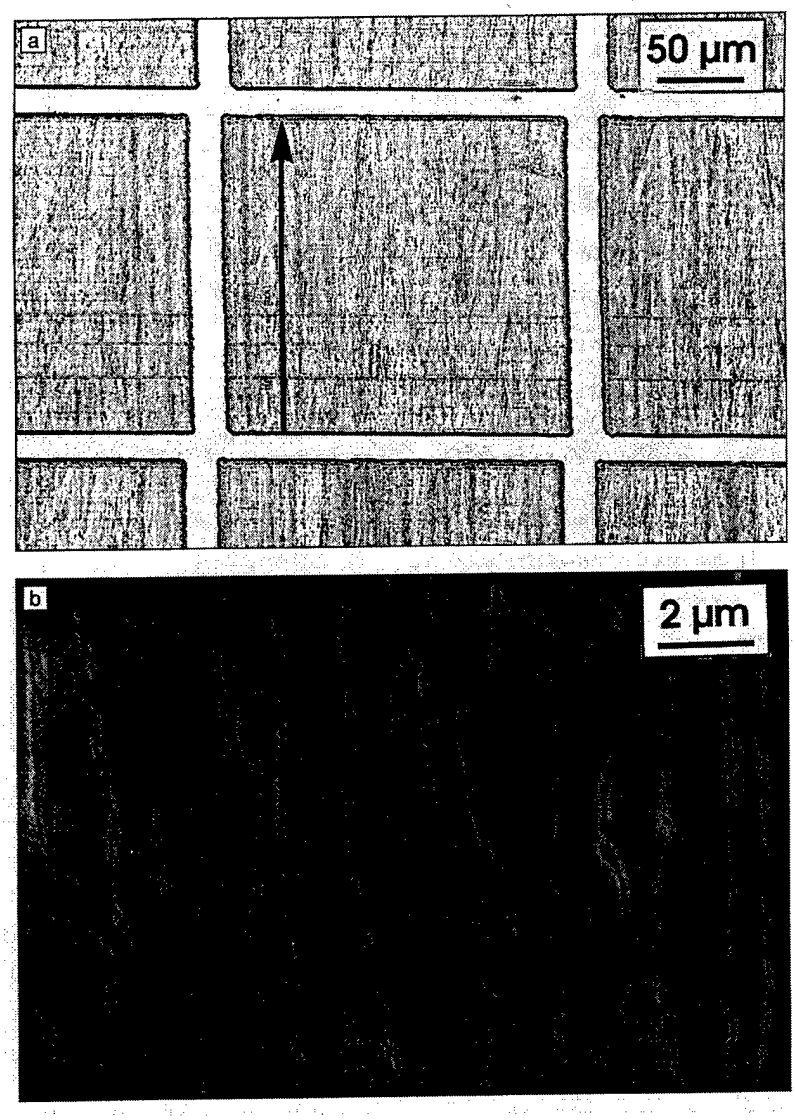


Fig. II.F1.2


Fig. II.F.1.3

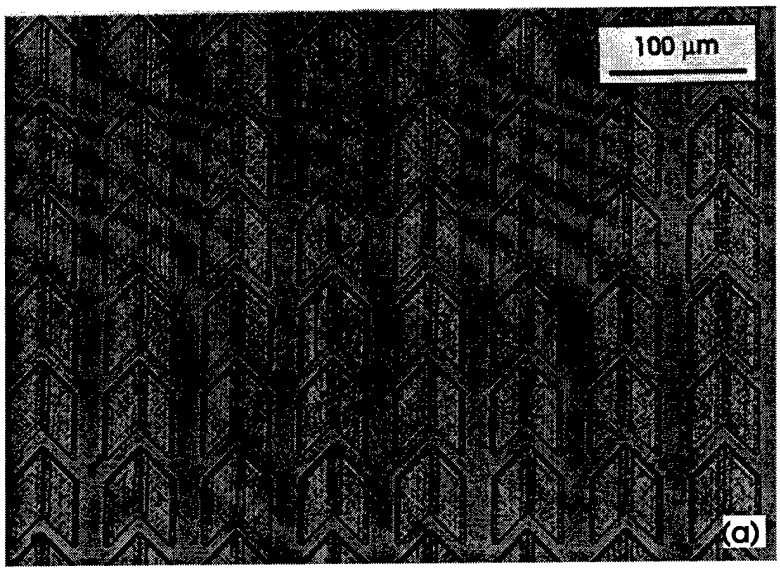


Fig. II.F2.1a

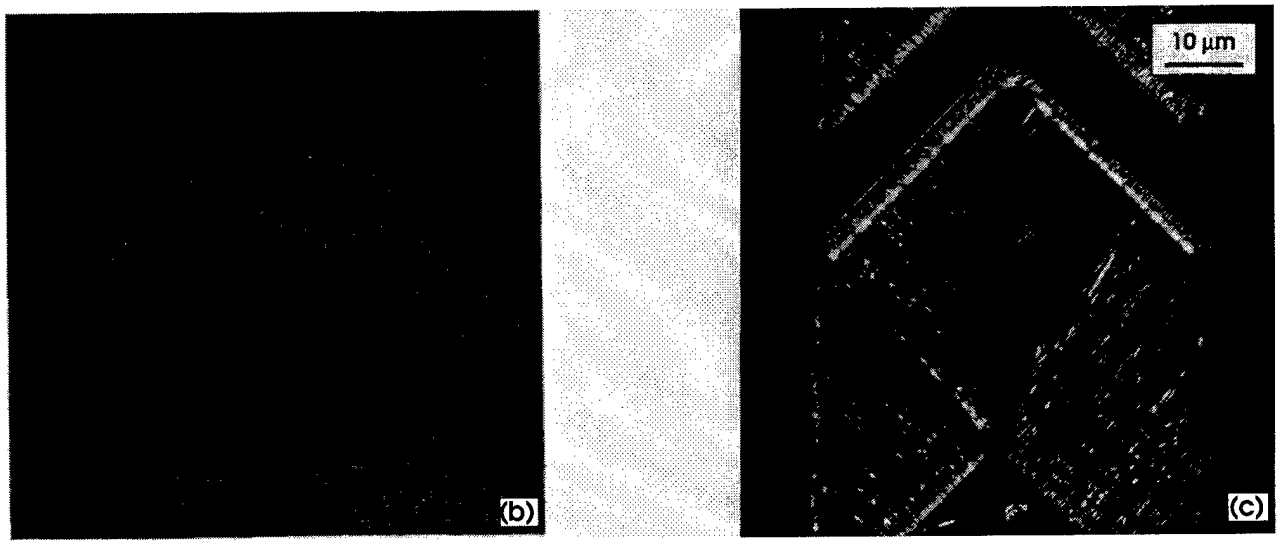


Fig. II.F2.1bc


Fig. F2.2a

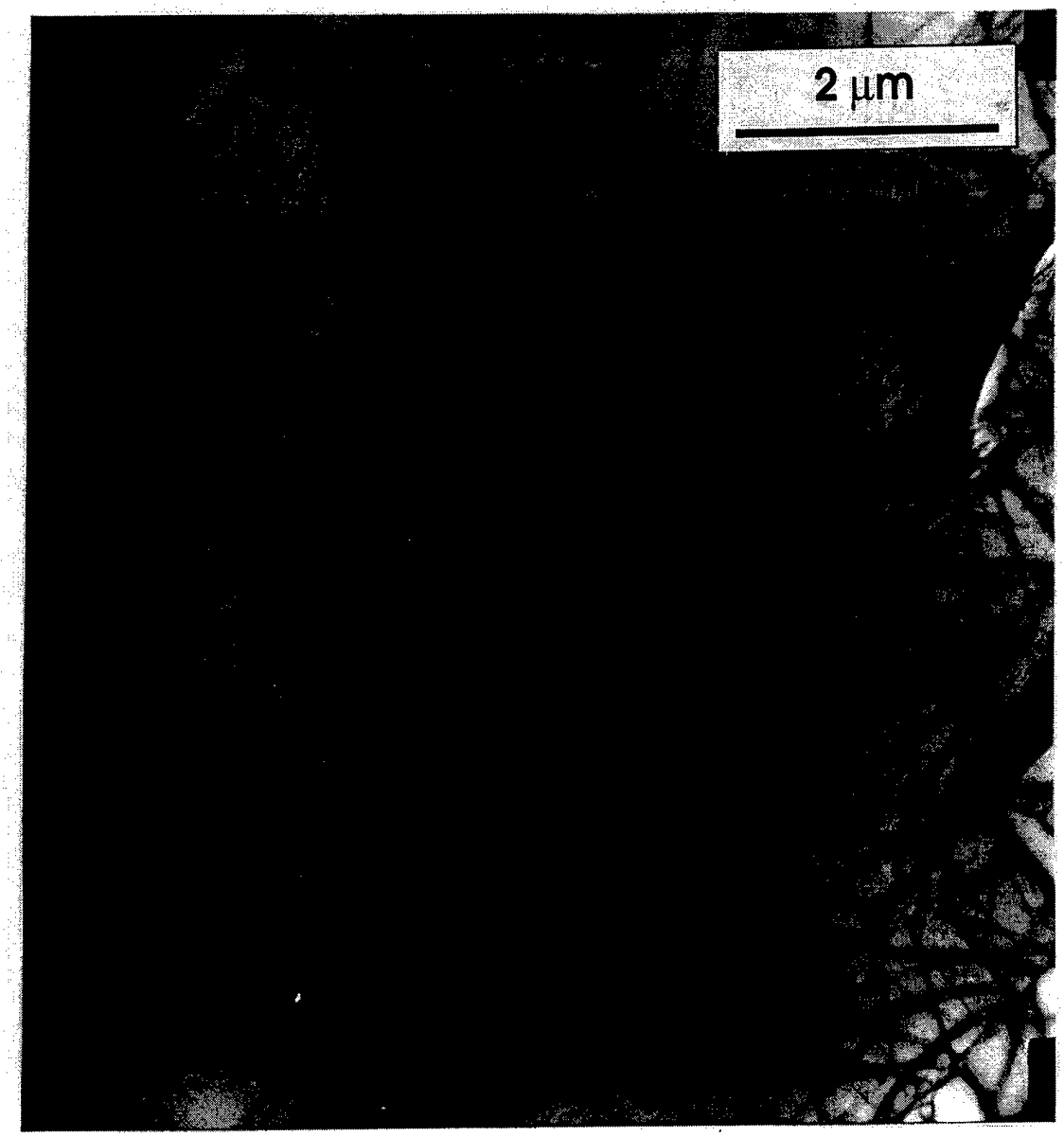


Fig. II.F2.2b

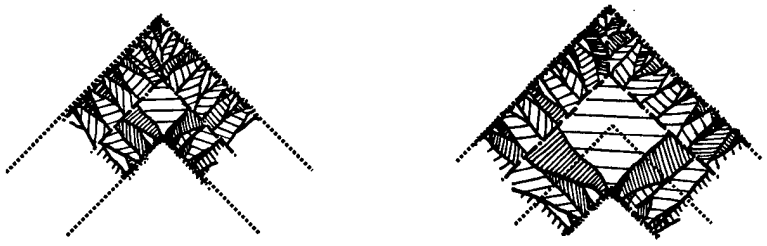


Fig. II.F2.3